CRDAC 12b

12 bit charge-redistribution DAC

Features

- f_s: max 160 MHz
- BW: 1 kHz – ½ f_s
- noise (1 kHz – 20 MHz): -72 dBV
- THD: -61 dBc
- area: 0.1 mm^2
- technology: 65 nm CMOS
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Applications

- l Baseband signal generation
- Inter-chip data communication
- Video baseband transmitting

General description

The CRDAC12b is a 12-bit charge-redistribution DAC.

The DAC is especially suited to discrete-time applications, where the output signal is sampled, but also works well in continuous-time applications.

The DAC has been optimized for high speed and low area. It has been designed for applications where DC transfer is not required.

This product is silicon verified

This product is still in development and all information in this datasheet is preliminary and subject to change

Block diagram

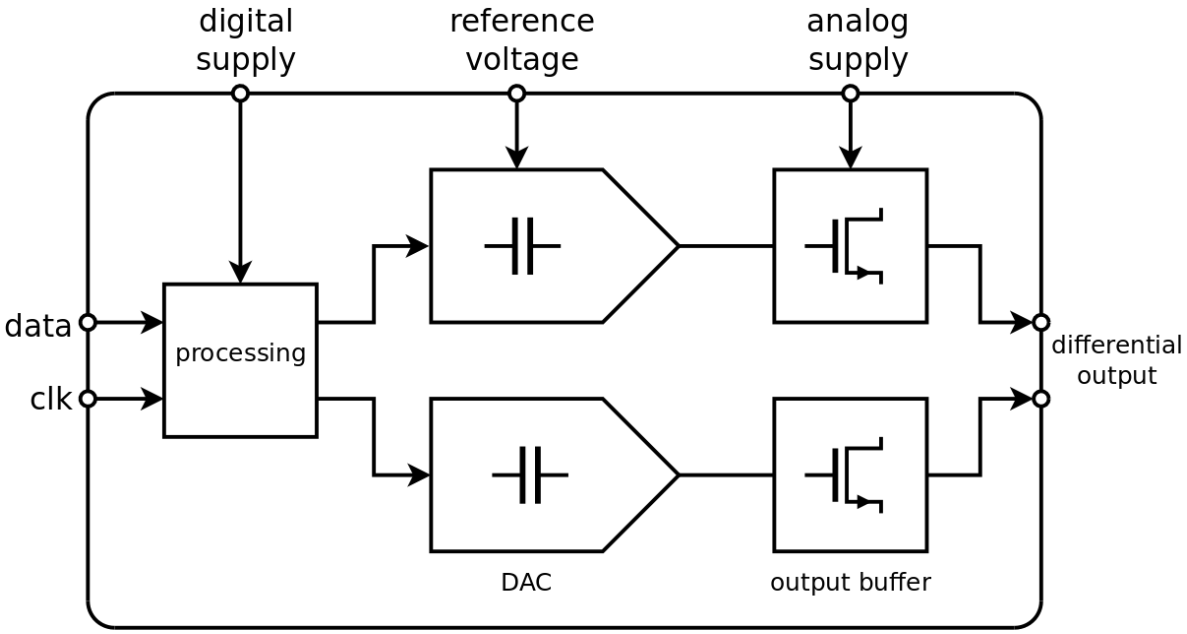

Figure 1: Block diagram

Ports list

Port name	Width	Description
Power, ground and reference ports		
$V_{dda}18$	1	1.8 V analog supply voltage for buffers
$V_{ref}12$	1	1.2 V reference (supply) voltage
$V_{ddd}12$	1	1.2 V digital supply voltage
Gnd	1	Common ground
Analog outputs		
Outp	1	Positive DAC output
Outn	1	Negative DAC output
Inputs (data and clock)		
Bx	12	Input data 12 bits
Clk	1	Clock input

Table 1: port function description

Specifications

Default test conditions

Digital supply voltage (V_{ddd})	1.2 V
Analog supply voltage (V_{dda})	1.8 V
IO supply voltage (V_{ddio})[1]	1.8 V
Reference voltage (V_{ref})	1.2 V
Clock frequency (f_{clk})	160 MHz
Input signal frequency	
Sampled-time measurements	55 MHz
Continuous-time measurements	5 MHz
Input signal amplitude	0 dBFS
Load impedance	2 kΩ // 5 pF (differential)
Ambient temperature (T)	25 °C

Specifications

Parameter	Description	Min	Typ	Max	Units
f_s	Sample rate		160		MHz
f_{clk}	Clock frequency		f_s		
V_{ddd}	Digital supply voltage		1.2		V
V_{dda}	Analog supply voltage		1.8		V
V_{ref}	Reference voltage		1.2		V
N	Input data width		12		bits
DC characteristics					
V_{cm}	Common mode output voltage		0.6		V
I_{ddd}	Digital supply current		<0.1		mA
I_{dda}	Analog supply current		14.9		mA
I_{ref}	Reference supply current		0.1		mA

Specifications (continued)

Parameter	Description	Min	Typ	Max	Units
AC Performance					
V_{out}	Output signal amplitude V_{in} = 0 dBFS		-7.4		dBV
BW	Input signal bandwidth [3] (ADC has high-pass transfer) Sampled-time measurements [4] Continuous-time measurements	 10^{-3} 10^{-3}		 60 20	MHz
R_{out}	Output resistance		140		Ω
THD	Total harmonic distortion V_{in} = 0 dBFS [2] Sampled-time measurement [4] Continuous-time measurement		 -61 -61		dBc
N	Noise floor 1 kHz-80 MHz, V_{in} = -48 dBFS Sampled-time measurement [4] Continuous-time measurement		 -72 -72		dBV
Implementation					
A	Chip area in 65nm CMOS		0.1		mm^2

Table 2: Specifications

Notes:

1. The test chip uses LVDS I/O signals, therefore an additional supply, Vddio (1.8V), is implemented on the test chip.
2. THD degrades with smaller input signals, due to crosstalk in test chip; see Figure 2.
3. See Figure 3.
4. Extracted from simulation

Typical Performance Characteristics

THD vs frequency

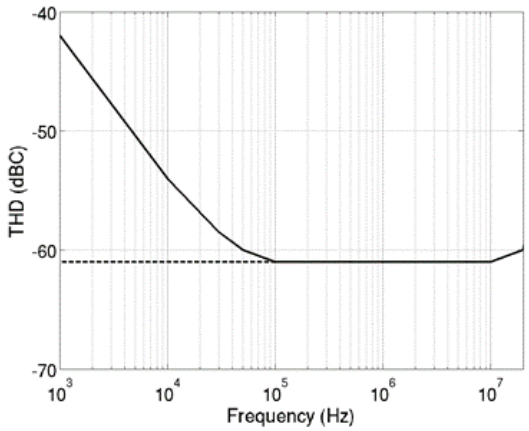

Figure 2: THD as function of frequency, V_{in} = 0 dBFS (the increase in THD for low frequencies is due to cross talk in the test chip; the dotted line indicates expected THD after resolving this issue)

Amplitude vs frequency

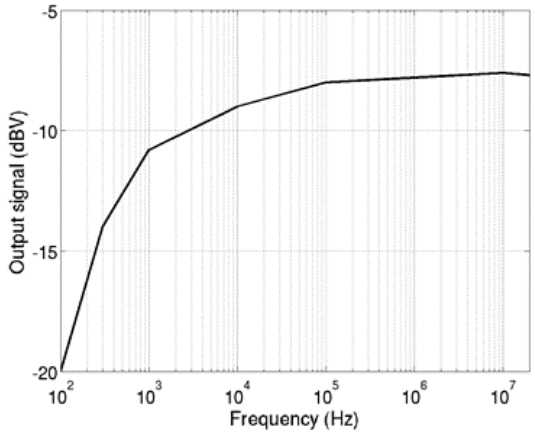

Figure 3: DAC output amplitude as function of frequency (V_{in} = 0 dBFS)

Typical Applications

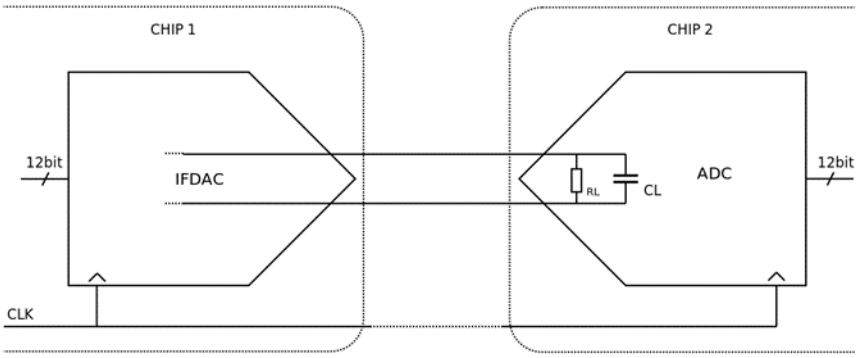

Figure 4: Typical IFDAC data communication application

Deliverables

The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

Revision history

Revision	Date	Reason for revision
F1	2011-07-05	Initial release
F2	2012-06-26	Removed “preliminary” status
F3	2017-07-20	Updated template

Table 3: Document revision history

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

or contact us at

Teledyne DALSA Enschede
Colosseum 28
7521 PT Enschede
the Netherlands
+31 (0)53-7990700
info.enschede@teledyne.com