Very-large-area CCD image sensors: concept and cost-effective research

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ABSTRACT

A new-generation full-frame 36x48 mm^2 48Mp CCD image sensor with vertical anti-blooming for professional digital still camera applications is developed by means of the so-called building block concept. The 48Mp devices are formed by stitching 1kx1k building blocks with 6.0 μm pixel pitch in 6x8 (hxv) format. This concept allows us to design four large-area (48Mp) and sixty-two basic (1Mp) devices per 6" wafer. The basic image sensor is relatively small in order to obtain data from many devices. Evaluation of the basic parameters such as the image pixel and on-chip amplifier provides us statistical data using a limited number of wafers. Whereas the large-area devices are evaluated for aspects typical to large-sensor operation and performance, such as the charge transport efficiency. Combined with the usability of multi-layer reticles, the sensor development is cost effective for prototyping.
Optimisation of the sensor design and technology has resulted in a pixel charge capacity of 58 ke$^-$ and significantly reduced readout noise (12 electrons at 25 MHz pixel rate, after CDS). Hence, a dynamic range of 73 dB is obtained. Microlens and stack optimisation resulted in an excellent angular response that meets with the wide-angle photography demands.

Keywords: CCD image sensors, digital still camera, quantum efficiency, pixel design, noise, dark current

1. INTRODUCTION

The need for large-area image sensors comes mostly from medical applications, photogrammetry and from the high-end professional digital still photography (DSC) market. In medical static X-ray imaging, typical requirements range from 24×24 mm^2 to 48×84 mm^2, but even larger imagers are used. In professional DSC applications, the compatibility with existing large-format lenses requires imagers as large as 36×48 mm^2. The high-end DSC applications govern the driving factors for the technology development. High resolution and dynamic range are two important parameters that define the image quality [1].

Designers and technologists are challenged to combine high quantum efficiency and large charge capacity with low dark current, good highlight-handling properties, and a high modulation transfer function. We approach this challenge by combining the vertical overflow drain pixel concept [2,3] that enables a high fill factor with a high transmittance of the optical stack. This report addresses the challenges and limitations to develop and manufacture large-area imagers in the context of cost-effective research. We will conclude with recent research achievements on novel stitchable full-frame CCD image sensors with a pixel pitch of 6.0 μm.

2. CCD IMAGE SENSOR DEVELOPMENT

2.1 Manufacturing challenges

Different wafer sizes are available on the market ranging from 6" wafers – typically used for professional imaging applications using CCD technology – up to 12" wafers for consumer CCD and CMOS applications. The upper limit for a large-area imager is governed by the size of the wafer. In order to manufacture a large area image sensor, a large wafer with a few large-area dice can be used or many small-area dice are placed side by side by means of the so-called butting

technique. A drawback of using large-area dice is the yield risk. The butting technique reduces this risk and reduces the system cost, however new challenges arise. Two major challenges that must be overcome involve mechanical engineering – the imager sensors must be positioned with an accuracy of a few micron – and image restoration.

Advanced semiconductor processes use 5:1 stepper lithography to define the resist patterns on the wafers. The reticle (or mask) used to project a layer of the design onto the wafer is typically a five times enlargement of the final dimensions of the resist pattern that will be formed on the wafers. These patterns define the geometry of the implants, interconnects, and contacts that will build the imager. The optical system of these steppers has a maximum size that generally limits the maximum chip size of typically 24×18 mm^2 on wafer level. Thus, the stepper defines the upper limit of the CCD imager size. Notice that this size corresponds to the advanced photo system (APS) size commonly used in consumer digital SLR cameras. This is half the size of conventional 35 mm film (24×36 mm^2).

In order to make larger imagers, the limitation of maximum exposure area of the stepper needs to be circumvented. Two solutions exist: the use of less advanced 1:1 lithography or applying stitching. In the case of the 1:1 lithographic method, the mask is projected 1:1 on the wafer. Hereby larger areas can be projected in a single exposure. Drawbacks of this technique are that the minimum dimensions are larger and the alignment accuracy between the different layers is less than obtained with 5:1 stepper lithography. Hence, the 1:1 lithographic technique is only useful for CCD processes that do not require small critical dimensions.

A preferred approach to overcome the maximum size of a single exposure of a 5:1 stepper, is to partition the design in blocks smaller than the maximum exposure area and then to stitch the design blocks together in the resist layer [4,5]. While the concept is very straightforward, this approach requires careful cooperation between the designer, the imager technologist, the mask manufacturer, and the litho specialist in the clean room.

Kreider *et al*. [4] reported a typical approach for stitchable designs. With this idea in mind, large CCD imagers with a resolution of nk × mk can be efficiently manufactured by splitting the design in 'building blocks' consisting of a 1k×1k imager array block, and separate blocks for the readout register, amplifiers, and interconnects. Using only one double reticle set makes a family of imagers. That is, the layers of the 1k×1k image block are placed on one set, and all the other smaller blocks are positioned on the other set. Figure 1 depicts a schematic illustration of a stitchable large-area image sensor.

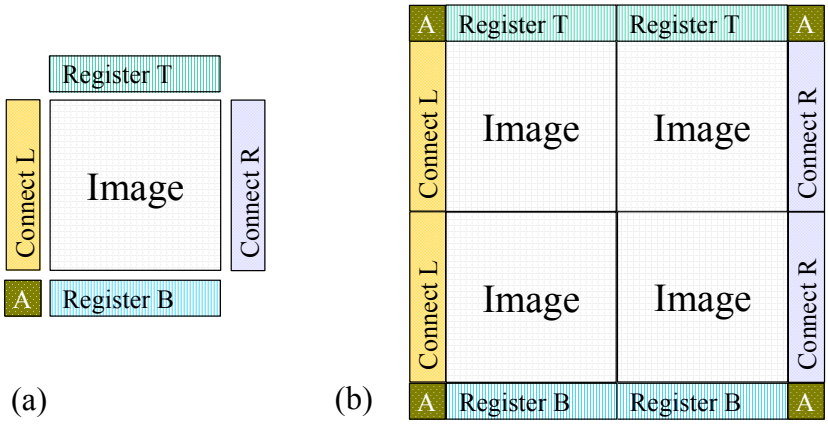

Figure 1: Illustration of the stitchable CCD architecture concept with (a) various building blocks and (b) a 2×2 stitched image sensor.

2.2 Cost-effective research for very-large-area CCD image sensors

The number of devices per wafer determines the limitation of the device and technology research on large-area sensors. In order to obtain enough data of different experimental designs, e.g., pixel and amplifier design concept, many sensors and thus wafers are required. Using multiple wafers and batches introduces the risk of wafer-to-wafer differences in the analysis. Although experiments can be performed on small area image sensors and hereby providing the statistical data, typical large area image sensor operation aspects, such as charge transport efficiency and the response time of the image

electrodes, can not be evaluated. Thus, we face the challenge to use the wafers and the wafer area in the most efficient way from economical and scientific points of view. We have applied the building block concept not only as a prove of principle for large-area CCD image sensor formation, but also to develop and to evaluate a new CCD imager – 6.0 µm pixel pitch – as successor of our 7.2×7.2 µm^2 imager used for DSC applications [6].

A newly developed concept is adapted, which combines many small and a few large dies on a single wafer, with the restriction that the imagers are made with the same reticle set. Figure 2a depicts a schematic layout of the wafer design, using the stitching concept as discussed in the previous section. An image of a processed 6" wafer is depicted in Fig. 3a. Four large-area (48Mp) and sixty-two small (1Mp) CCD image sensors are designed on a single wafer. Each image sensor has one of the stitchable amplifier blocks, Amp mix i, containing four amplifiers. The wafer includes several process control modules (PCMs) placed between the small area imagers. As Fig. 2 indicates, the all-gates-pinning (AGP) concept is applied to part of the 1Mp CCD image sensors, which results in a drastic reduction of the dark current [7,8]. On a single wafer and between different wafers, variants in design, process, and dope implants are used in order to optimize the AGP design. Although more small area devices are designed on the wafer as observed from Fig. 2, the number of usable imagers is reduced to sixty-two due to wafer edge effects. The small and large dies are composed of the same building blocks for the image area, readout registers, amplifiers, and interconnects as proposed in the previous section. The use of multi-layer reticles reduces the cost for a reticle set for prototyping significantly. The large die is realized by stitching the small building blocks many times. However, this does not prevent these devices to be used for early prototyping in the customer's application.

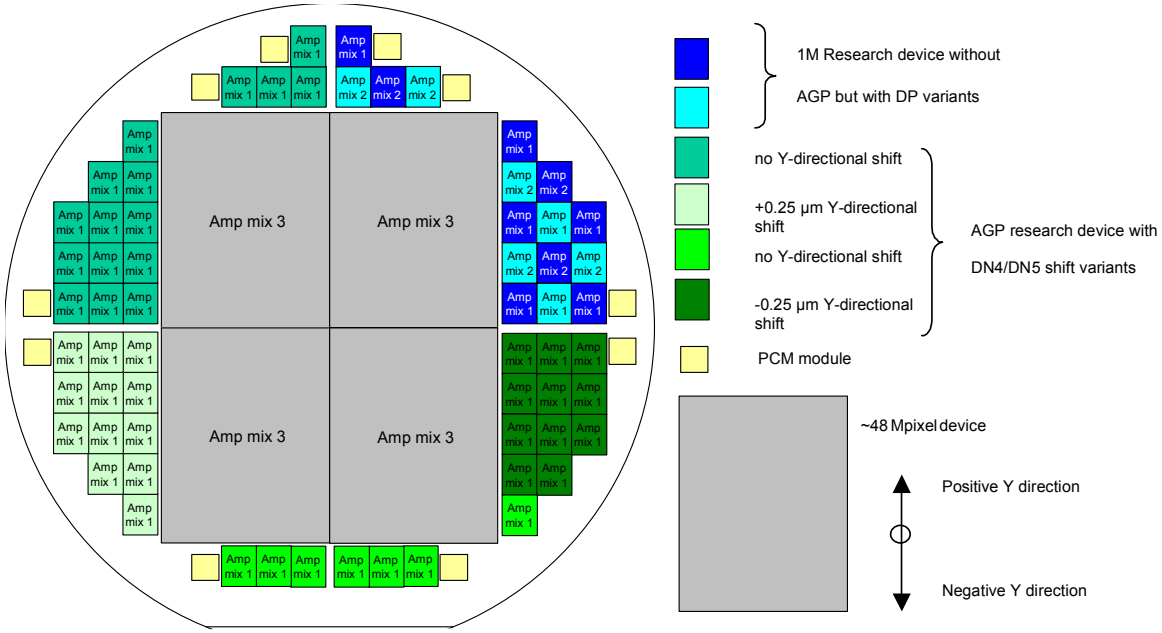

Figure 2: (a) Schematic wafer layout. Different amplifiers – indicated with Amp mix i – and imager configurations are designed. The abbreviations DP and DN stand for the p and n dope implants, respectively.

The example in Fig. 2 was used to develop new building blocks and improved CCD technology for imagers for professional DSC applications. On the wafer, various experiments are designed – this accounts for the image area, registers, and the amplifiers. Besides the on-wafer experiments, the batch has wafer-to-wafer variations. That is, new technological concepts are introduced for optical response and noise improvement. Both small and large sensors have two horizontal bi-directional readout registers and four amplifiers.

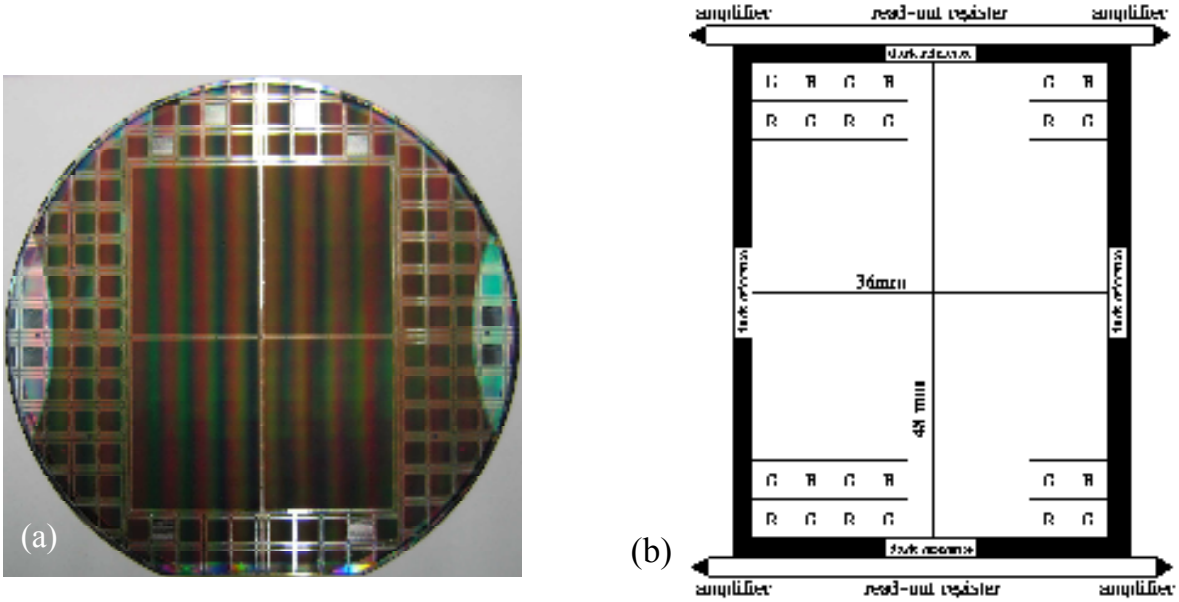

Figure 3: (a) Photograph of a processed wafer using the building block concept, with the layout as depicted by Fig. 2. (b) Schematic layout of a 48Mp full-frame CCD image sensor with Bayer color pattern.

Figure 3b shows a schematic layout of the new 48Mp 36×48 mm^2 device. The bottom readout register is a 3-phase register while the upper one is a 4-phase (quasi 2-phase) register. The large sensor has four identical on-chip amplifiers (one at each corner), which has three source followers. This amplifier is well evaluated previously and is used as a reference that is required for the overall evaluation. The small device has an identical concept and is supplied with the reference amplifier and experimental types. In total, four experimental amplifiers (using three or four source followers) are designed. Which on-chip amplifier is used depends on the location of the small imager on the wafer, see Fig. 2.

2.3 Pixel development

DALSA developed a technology that combines simplicity of design and technology with high performance. This technology uses two thin 'membrane' transparent layers of poly-silicon to define the pixel electrodes and two layers of metal for the interconnections [9]. By combining the concept of vertical anti-blooming (VAB) [2,3] – also called vertical overflow drain – with a high fill factor (even without microlenses) and a high transmittance of the optical stack, a pixel is developed that combines a high quantum efficiency, large charge capacity with low dark current, good highlight handling properties, and a high modulation transfer function.

In the VAB concept, the CCD channel is formed by n-channel implant on a p-well in a n-type substrate. This VAB structure is a preferred implementation for buried-channel CCD imagers that need to combine overexposure control with electronic shuttering. Figure 4a shows the potential profile as a function of depth in the silicon, under an integrating and a blocking gate. The collection depth for electrons, which are generated by incident photons inside the silicon substrate, is governed by the location of the local potential minimum. These electrons are subsequently collected in the potential well. This collection depth, in combination with the penetration depth of photons in silicon, results in a response curve as a function of wavelength similar to that of the human eye. When a highlight in the scene generates more electrons than can be stored in the pixel, the excess charge is drained toward the substrate and does not bloom into neighboring pixels, since the potential barrier to the substrate is lower than the potential barrier to a neighboring pixel.

As depicted by the simulation results, see Fig. 4b, the electron collection region has sufficient distance from the Si-SiO_2 interface to avoid charge trapping. The vertical anti-blooming concept also results in a low dark current, since any dark current generated in bulk of the device, in the n-substrate below the potential minimum, is not collected in the pixel.

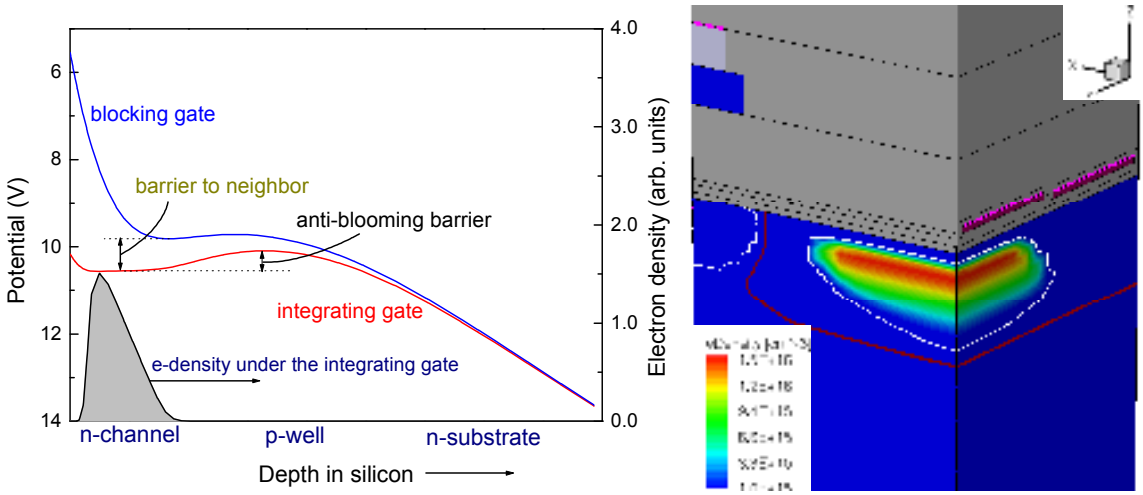

Figure 4: (a) Potential profiles of a filled image pixel with vertical anti-blooming – the blocking and integrating gate – and (b) device simulation of a saturated pixel – one quarter. The pixel architecture is depicted in Fig. 5.

In order to compensate the 30% size reduction, adjustments in the design and technology are required. This includes an improvement of the quantum efficiency by means of deposition of an anti-reflective nitride layer on the poly-silicon gate electrodes. Furthermore, gapless microlenses on top of the color filter pattern are used. The microlenses are optimized for wide-angular response and will minimize optical cross talk. Figure 5 depicts a schematic illustration of the architecture of the 7.2×7.2 µm^2 pixel [6] and its 6.0×6.0 µm^2 successor.

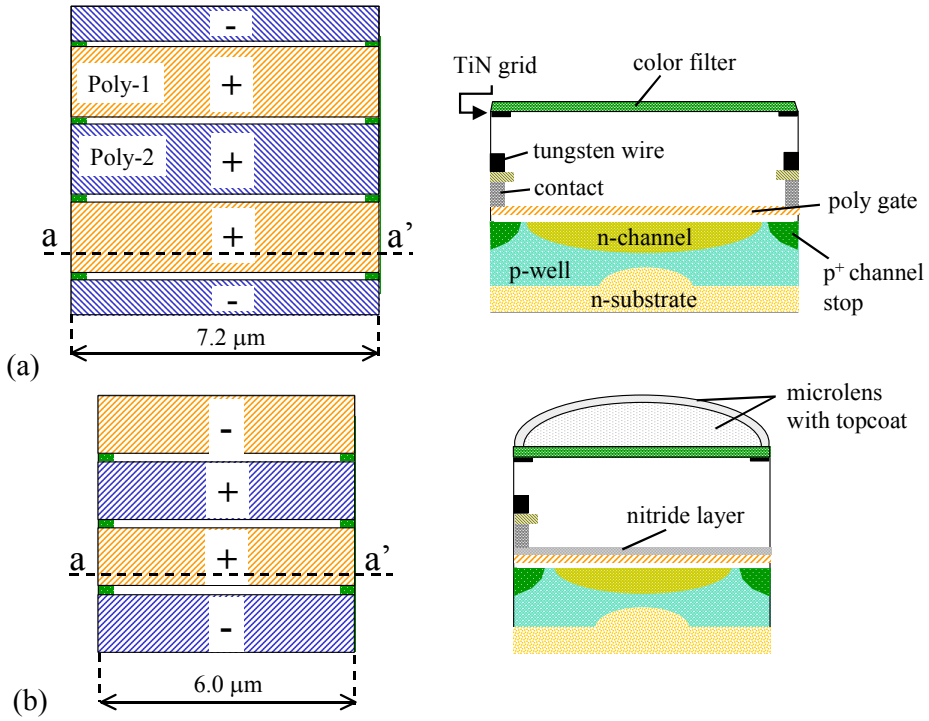

Figure 5: Schematic illustration of the previous (a) and the present (b) pixel architecture. The cross-section is along line a-a'. The 7.2×7.2 µm^2 CCD imager [6] operates with three integrating gates (indicated with the + sign) and one blocking gate (- sign), the so-called three-one mode, whereas a two-two mode is used for the 6.0×6.0 µm^2 imager.

3. SENSOR EVALUATION

The size reduction of 30% directly affects the effective potential well of the pixel. In order to preserve the pixel charge capacity and optical response, we must adapt the dope implants. To evaluate the novel pixel architecture we have evaluated small as well as large-area image sensors coming from different locations on the wafer and from different wafers. The latter is used for the evaluation of imagers with the AGP concept – we used dope implant variations for optimization – and to evaluate the optical response of monochromatic imagers and those with color filters.

The wafer layout as depicted in Fig. 2 allows numerous design and technological experiments. Here we restrict ourselves to non-AGP CCD image sensors, which we can compare with the preceding full-frame CCD image sensor with a pixel pitch of 7.2 µm [6].

3.1 Pixel linearity and charge capacity

One of the key features of digital image sensors is the dynamic range of the pixel. Although this range is governed by the maximum charge capacity of the pixel, in reality a restriction is induced by linearity of the pixel's optical response. That is, the light response of the pixel should be linear up to saturation. For the evaluation we used a white light emitting diode (LED) with a broad emission spectrum combined with an infrared filter in front of the CCD image sensor. During the measurements, the integration time of the CCD image sensor is fixed and the illumination time is varied. The LED has a fast response, in other words a negligible on-off delay, such that the illumination time is well known. To ensure that the imager is not illuminated during charge transport due to timing jitter, a 2 ms readout delay is used.

Figure 6 depicts experimental results obtained for different voltages on the integrating gates. The applied voltage on the blocking gates is set to zero. The maximum charge capacity of the 6.0 µm pixel depends linearly on the applied gate voltage. For a gate setting of 12.2 V a pixel capacity of approximately 58×10^3 electrons is measured. This number is comparable with the capacity of our preceding large-area image sensor with a pixel pitch of 7.2 µm [6].

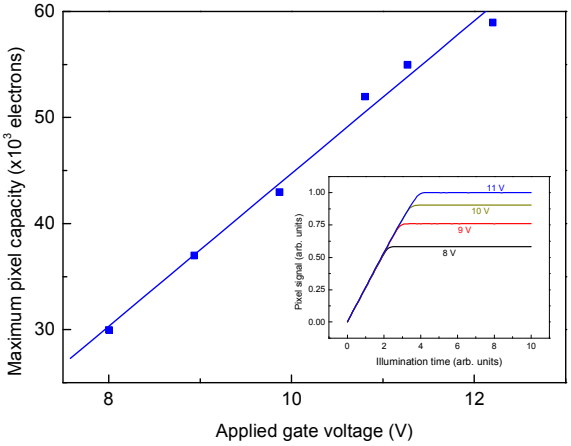

Figure 6: Maximum charge capacity as a function of the applied gate voltage. The inset depicts linearity measurements for different gate voltages.

3.2 Optical response

To obtain a better match of the refractive indices of the layers within the optical stack, a nitride layer is deposited on top of the poly-silicon electrodes. Spectral response measurements allow us to investigate the effect of the technology change. A broad spectral light source is used in combination with a 0.275 m triple grating monochromator to illuminate the image sensor with monochromatic light. Figure 7a depicts the spectral response of two color CCD imagers with a pixel pitch of 6.0 and 7.2 µm. A significant improvement of the quantum efficiency is noticed, as is emphasized by the inset. The improved optical response is due to the introduction of the nitride layers and the use of microlenses.

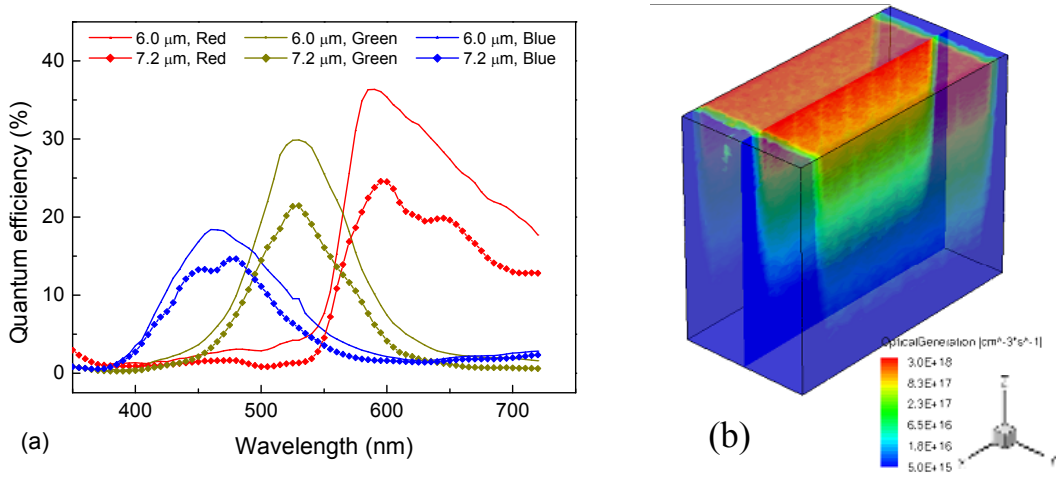

Figure 7: (a) Quantum efficiency spectrum of the 7.2×7.2 μm^2 CCD imager and its 6.0×6.0 μm^2 successor, both with the Bayer color filter pattern. (b) Optical simulation result of half a pixel for a wavelength of 500 nm, within the silicon substrate directly under the gates.

Optical simulations are performed to analyze the optical generation of electron-hole pairs with the silicon substrate, see Fig. 7b. Notice that the majority of the carriers are generated within the potential well of the image sensor. Combing the experimental data from the different wafers, and thus different image sensors, we obtain a better insight of the sensor performance.

3.3 Angular response

The angular response of an image pixel is governed by the optical properties of the optical stack deposited on the electrodes and by the light sensitive (or active) area within the silicon underneath the gates. That is, the 'width' of the active area varies with depth and thus the angular response varies with optical wavelength. With respect to the optical properties of the stack, the refractive indices of the materials in the 'blue region' are higher than those in the 'red region'. Hence, blue-light will be deflected more toward the center of the image pixel than light with a larger wavelength. Figure 8 depicts a schematic illustration of the pixel array configuration. For the angular evaluation a white LED and an infrared filter is used. A good angular response is observed for all colors. The experimental results as depicted in Fig. 8 show that the tungsten bars, see Fig. 8, do not influence the angular response due to the on-top microlenses.

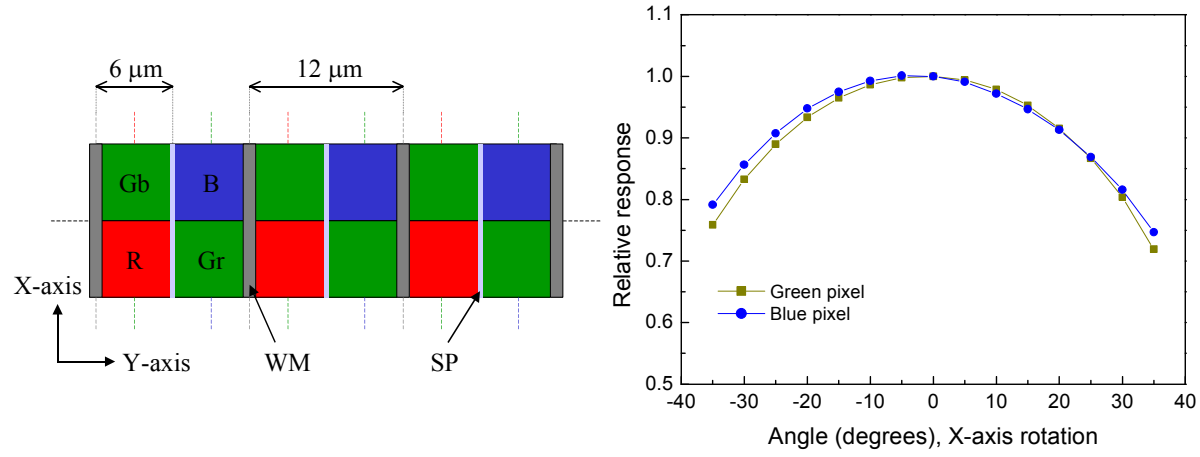

Figure 8: Schematic layout of the pixel design showing the channel stops (SP-lines) and the tungsten bars (WM). The experimental data is obtained for rotation around the X-axis.

3.4 Dark current

Due to the large number of pixels in the large-area CCD image sensor, the readout time becomes significant even with a horizontal (vertical) clock frequency of 25 MHz (50kHz). To preserve high-quality images the dark noise level must be low. Dark current is also a very important noise source that can become significant for long exposure times. Although dark noise generation is an intrinsic property of silicon based devices, discrimination can be made between bulk and surface dark current. The latter is generated at the Si-SiO_2 interface and dominates in general.

For the evaluation, dark images are taken at different temperatures and with different integration times. The experimental results are depicted in Fig. 9. Based on these results the dark current is deduced, see Fig. 9b. The experimental fits reveal that the noise level doubles every 9.3 degrees.

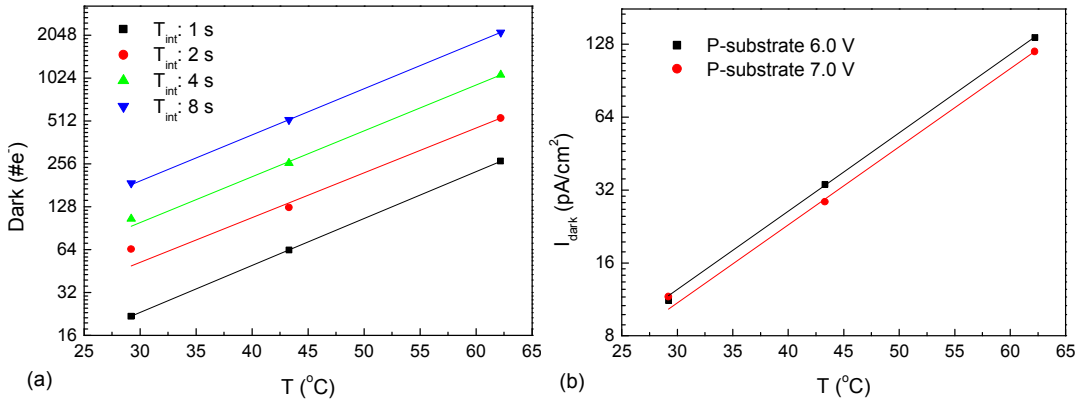

Figure 9: (a) Dark noise (number of electrons) as a function of temperature for different integration times. (b) Dark current as a function of temperature determined for different vertical barrier settings.

Results of the measurement series with two different settings of the barrier to the substrate are depicted in Fig. 9b. Increase of the applied voltage to the p-well results in an increased pinning layer. The latter causes the reduced dark current. That is, the contribution of the surface dark current becomes less. Dark noise generation at the Si-SiO_2 interface is also suppressed in imagers applied with the AGP concept [7,8]. Preliminary measurement results indicate that sensors with the new AGP design perform equally with our previous AGP based CCD image sensors [8], which have a dark current of 0.6 pA/cm^2 at 35°C. Evaluation of our new AGP concept is beyond the scope of this paper and will be reported elsewhere.

3.5 Amplifier performance

The on-chip amplifier forms the bridge between the image sensor and the outside world. Here the charge package is converted into an output voltage. Thus, the amplifier plays a crucial role within the whole chain. Therefore the performance of the amplifier must be thoroughly evaluated. Changes in the wafer processing can result in altered characteristics. Before changes are applied, the impact on the on-chip amplifier is taken into consideration. One of these changes is the additional nitride processing. Although not mentioned above, the processing has a positive effect on the noise spectrum of the on-chip amplifier, as depicted in Fig. 10a. The readout noise of the triple-source follower amplifier decreased from 17 down to 12 electrons after CDS processing at 25 MHz pixel frequency, as deduced from the photon transfer curve depicted in Fig. 10b. The bandwidth is maintained at 125 MHz, which is required for good color separation. In addition, the amplifier conversion factor remained high and had a value of approximately 38 μV/e-.

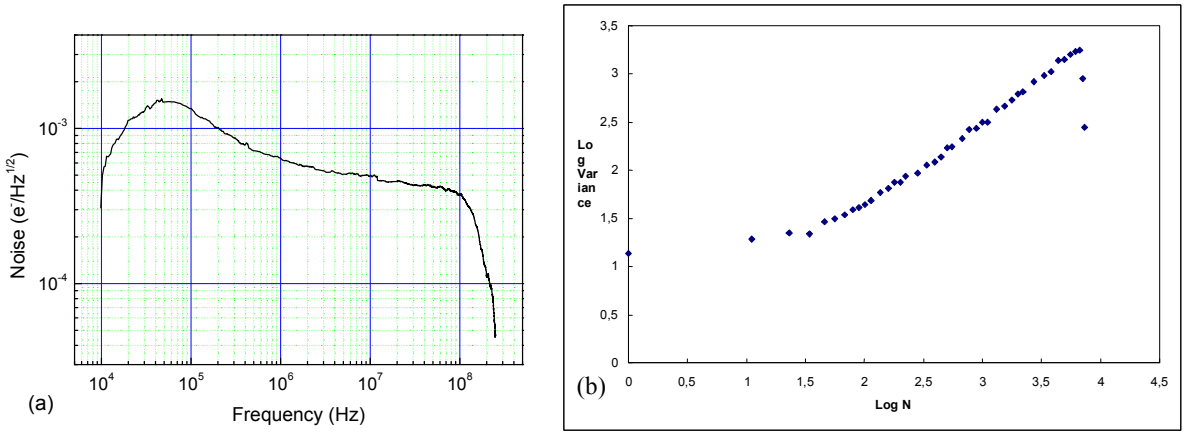

Figure 10: (a) Noise spectrum of the reference on-chip amplifier and (b) the photon shot noise curve, using 6 dB gain and a total integration time of 75 ms.

SUMMARY

An overview of cost-effective research is presented, which allows fabrication of very-large-area CCD image sensors with enough data for statistical analysis. Using the stitchable building block concept also allows research flexibility within one wafer batch. Hence, a significant cost reduction can be obtained. Large-area CCD image sensors for DSC applications are fabricated using smaller building blocks.

In order to meet with the sensor requirements, the design of our novel CCD image sensor with a 6.0 μm pixel pitch is changed with respect to the design of the 7.2×7.2 μm^2 predecessor. Optimization of the sensor design and technology has resulted in a significantly improved performance of the large-area CCD image sensor, in spite of the 30% size reduction. With a maximum charge capacity of 58×10^3 electrons and a noise level of 12 electrons after CDS processing, a dynamic range of 73 dB is obtained.

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