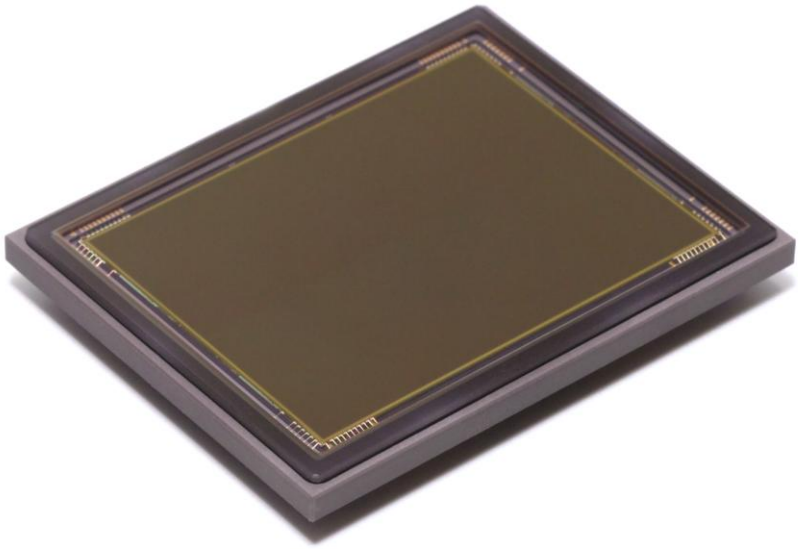
DATA SHEET



FTF9168M

60M Monochrome Full-Frame CCD Image Sensor

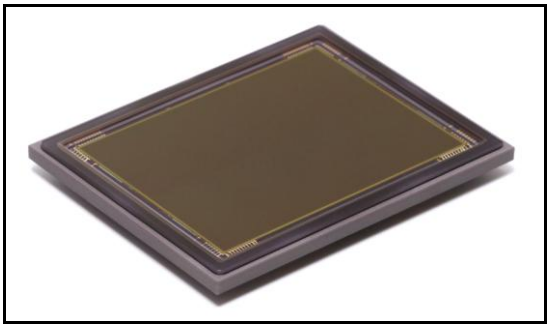
Product Specification May 30, 2013

Teledyne DALSA
Professional Imaging

TELEDYNE DALSA
Everywhereyoulook™

60M Monochrome Full-Frame CCD Image Sensor FTF9168M

- **Large Image format (53.8 x 40.3 mm^2)**
- **60M active pixels (8956H x 6708V)**
- **Monochrome pixel optimized for wide sensitivity range (blue to near-IR)**
- **Microlenses for high fill factor and high response uniformity with wide angular response**
- **Progressive scan**
- **Excellent antiblooming**
- **Fast variable electronic shuttering**
- **Square pixel structure**
- **High dynamic range (>70dB)**
- **High sensitivity**
- **Perfectly matched to photogrammetry spectrum**
- **Low dark current and low fixed pattern noise**
- **Low readout noise**
- **Data rate up to 25 MHz per output**
- **Mirrored and split readout**
- **RoHS compliant**



Description

The FTF9168M is a 60M-pixel, large-format, monochrome, full-frame CCD imager for use in the most demanding aerial photography and photogrammetry applications The image area with 8956 x 6708 active pixels of 6x6 μm^2 has a 4:3 aspect ratio. The active image area dimension is 53.736 x 40.248 mm^2. The four-phase pixel concept is perfectly matched to the requirements of forward motion compensation (FMC).

The pixels are optimized for a wide spectral range (blue to near-IR) with excellent response uniformity. A high fill factor (> 95%) in combination with a very wide angular response is achieved by the use of proprietary on-chip micro-lenses. The vertical Anti-blooming (VAB) structure ensures excellent highlight handling, fast electronic shuttering and high MTF.

Vertical and horizontal binning is supported to offer the option of exchanging resolution for sensitivity and/or readout speed.

The device has four identical low-noise output amplifiers, one at each corner of the chip, to allow simultaneous readout through one, two or four outputs. The Dynamic Range is >11 true bits at 60°C and 25 MHz pixel frequency.

The device is assembled in a hermetically sealed PGA package.

Device structure

Optical size:	53.736 mm (H) x 40.248 mm (V)		
Chip size:	55.680 mm (H) x 41.188 mm (V)		
Pixel size:	6.0 μm x 6.0μm		
Active pixels:	8956 (H) x 6708 (V)		
Total no. of pixels:	9004 (H) x 6798 (V)		
Optical black pixels	Left: 20	Right: 20	
Dummy edge pixels	Left: 4	Right: 4	
Dummy lines:	Bottom: 33	Top: 33	
Optical black lines:	Bottom: 8	Top: 8	
Dummy edge lines:	Bottom: 4	Top: 4	
Dummy register cells	Left: 29	Right: 29	

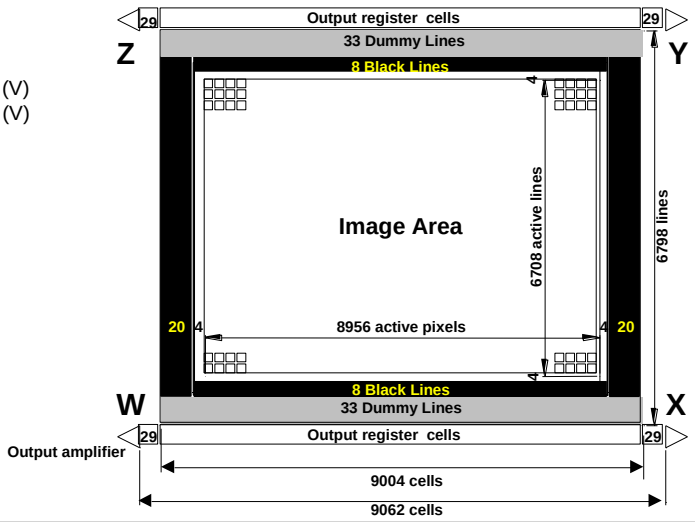


Figure 1: Device Structure

Architecture of the FTF9168M

The optical centers of all pixels in the image section form a square grid. The charge is generated and integrated in this section. The pixels use a four-phase structure (A1, A2, A3, A4), allowing quarter-pixel accuracy in forward motion compensation. The output registers located below and above the image section allow split readout (L-R) and are controlled by three-phase clocks (C1, C2, C3). After the integration time, the image charge is shifted one line at a time to either the upper or lower register or to both simultaneously, depending on the readout mode. The left and right half of each register can be controlled independently. This enables either single or multiple read-out. During vertical transport, the C3 gates separate the pixels in the register. The central C3 gates of the lower and upper registers are part of the left half of the sensor (W and Z quadrants respectively).

Vertical binning is achieved by adding lines in the registers. Each register contains a summing gate (SG) at both ends that can be used for horizontal binning (see figure 2). The charge-to-voltage conversion is performed by a three-stage source follower amplifier (4 in total). The charge-to-voltage conversion node is reset to reset-drain voltage (RD) by pulsing the reset gate (RG). The amplifier power supply is SFD, the ground terminal is SFS. VNS and VPS are the bias voltages for the n-type substrate and for the CCD p-well, respectively.

IMAGE SECTION	
Image diagonal (active video only)	67.14 mm
Aspect ratio	4:3
Active image width x height	53.736 x 40.248 mm^2
Pixel width x height	6.0 x 6.0 μm^2
Fill factor	95%
Image clock pins	16 (4x4) pins (A1...A4)
Capacity of each clock phase	300 nF
Total number of lines	6798
Number of active lines	6708
Number of edge lines	8 (=2x4)
Number of black lines	16 (=2x8)
Number of dummy lines	66 (=2x33)
Total number of pixels per line	9004
Number of active pixels per line	8956
Number of edge pixels per line	8 (2x4)
Number of black reference pixels per line	40 (2x20)

OUTPUT REGISTERS	
Number of output registers	2 (T /B), each with two output amplifiers (L/ R)
Total number of register cells per register	9062
Number of register cells below/above image	9004
Number of dummy register cells	58 (2x29)
Output register horizontal transport clock pins	6 pins per register (C1...C3)
Capacity of each C-clock phase	200 pF per pin
Overlap capacity between neighboring C-clocks	40 pF
Output register Transfer Gate	1 pin per register (TG)
Capacity of each TG	15pF
Output register Summing Gates	1 pin per output (SG)
Capacity of each SG	15pF
Reset Gate clock phases	1 pin per output (RG)
Capacity of each RG	15pF
Output amplifier type	Three-stage source follower

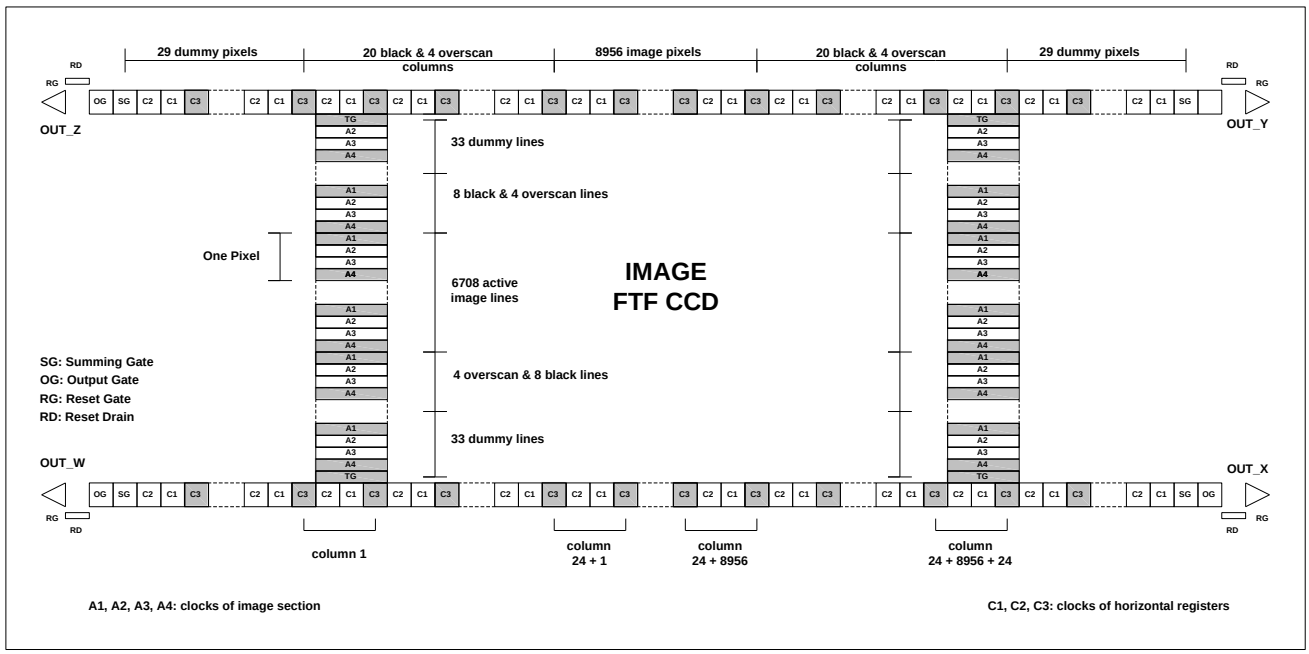


Figure 2: Detailed internal device structure

Operating Conditions

Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS[1]	MIN	MAX	UNIT
GENERAL:			
Storage temperature	-40	+80	°C
Ambient temperature during operation	-20	+60	°C
Voltage between any two gates	-20	+20	V
DC current through any clock (absolute value)	-0.2	+0.2	µA
OUT current (no short circuit protection)	0	+10	mA
VOLTAGES IN RELATION TO VPS:			
VNS, SFD, RD	-0.5	+30	V
VCS, SFS	-8	+5	V
All other pins (except RG)	-20	+25	V
VOLTAGES IN RELATION TO VNS:			
SFD, RD	-15	+0.5	V
SFS, VPS	-30	+0.5	V
All other pins (except RG)	-30	+0.5	V
VOLTAGES IN RELATION TO SFD:			
RD	-5	0	V
RG Voltage	0	+30	V

[1)] During Charge reset it is allowed to exceed maximum rating levels in relation to VNS, according to the specified DC voltage settings and AC clock level conditions.

DC Voltage Settings

DC CONDITIONS[1, 2]		MIN [V]	TYPICAL [V]	MAX [V]	MAX [mA]
VNS[3]	n-substrate	20	adjusted	28	15
VPS	p-well	5.5	6	6.5	15
SFD	Source Follower Drain	19.5	20	20.5	5
SFS	Source Follower Source	0	0	0	1
VCS	Current Source	0	0	0	–
OG	Output Gate	5.0	6.0	7.0	–
RD	Reset Drain	19.5	20	20.5	–

[1] All voltages in relation to SFS; typical values are according to test conditions.
[2] Power-up sequence: VNS, SFD, RD, VPS, all others. The difference between SFD and RD should not exceed 5V during power up or down.
[3] To set the VNS voltage for optimal Vertical Anti-blooming (VAB), it should be adjustable between minimum and maximum values
[4] Maximum current for each amplifier
.

Note on Voltage Settings

Since the AC signals for operating the horizontal register (register clocks C1-C2- C3, summing gate SG) and the output stage (reset gate RG) are analog signals for the CCD, the optimal voltage settings can be influenced by the waveforms of these signals, which in turn depend on the layout and schematics of the camera electronics. Thus the optimal value of all DC biases mentioned can deviate up to +/-1V from the ‘typical’ values mentioned in the data sheets depending on the precise implementation of the hardware around the sensor. All DC and AC voltages settings in the following tables are measured on sensor pins.

AC Clock Level Conditions

The following voltages should be applied for operating the sensor.
A clocking scheme of 2 gates integrating and 2 gates blocking should be used.

AC CLOCK LEVEL CONDITIONS[1]	MIN	TYPICAL	MAX	UNIT
IMAGE CLOCKS/ TRANSFER GATES[2]:				
A-clock amplitude during integration and hold (integration with 2 gates high)		11		V
A-clock amplitude during vertical transport (readout and FMC) (duty cycle=5/8) [3]		13.5		V
A-clock low level	-	0	-	V
Charge Reset (CR) level on A-clock[4]	-0	0	-	V
OUTPUT REGISTER CLOCKS:				
C-clock amplitude (duty cycle during hor. transport=3/6)	4.75	5	5.25	V
C-clock low level	2.25	2.75	3.75	V
Summing Gate (SG) amplitude	4.75	5	5.25	V
Summing Gate (SG) low level	3.75	4.25	4.75	V
OTHER CLOCKS:				
Reset Gate (RG) amplitude		5		V
Reset Gate (RG) low level	16.5	17	17.5	V
Charge Reset (CR) pulse on Nsub[4]	0	5	5	V

[1] All voltages in relation to SFS; typical values are according to test conditions
[2] Transfer Gate should be clocked as A1 during normal transport or held low during a line shift to sub-sample image
[3] Three-level clock is preferred for maximum charge; the swing during vertical transport should be 3V higher than the voltage during integration
A two level clock (typically 10V) can be used if a lower maximum charge handling capacity is allowed
[4] Charge Reset is achieved by applying the typical A-clock low level to all image clocks together with an additional Charge Reset pulse on VNS

Timing diagrams (for default operation)

AC CLOCK CHARACTERISTICS	MIN	TYPICAL	MAX	UNIT
Horizontal frequency (1/Tp)[1]	-	25	-	MHz
Vertical frequency	-	50	-	kHz
Charge Reset (CR) time	10	Line time	-	µs
Rise and fall times: image clocks (A)	10	20	-	ns
register clocks (C)[2]	3	5	1/8 Tp	ns
summing gate (SG)	3	5	1/8 Tp	ns
reset gate (RG)[3]	-	3	1/8 Tp	ns

[1] Tp = 1 clock period
[2] Duty cycle = 3/6
[3] Duty cycle = 1/6

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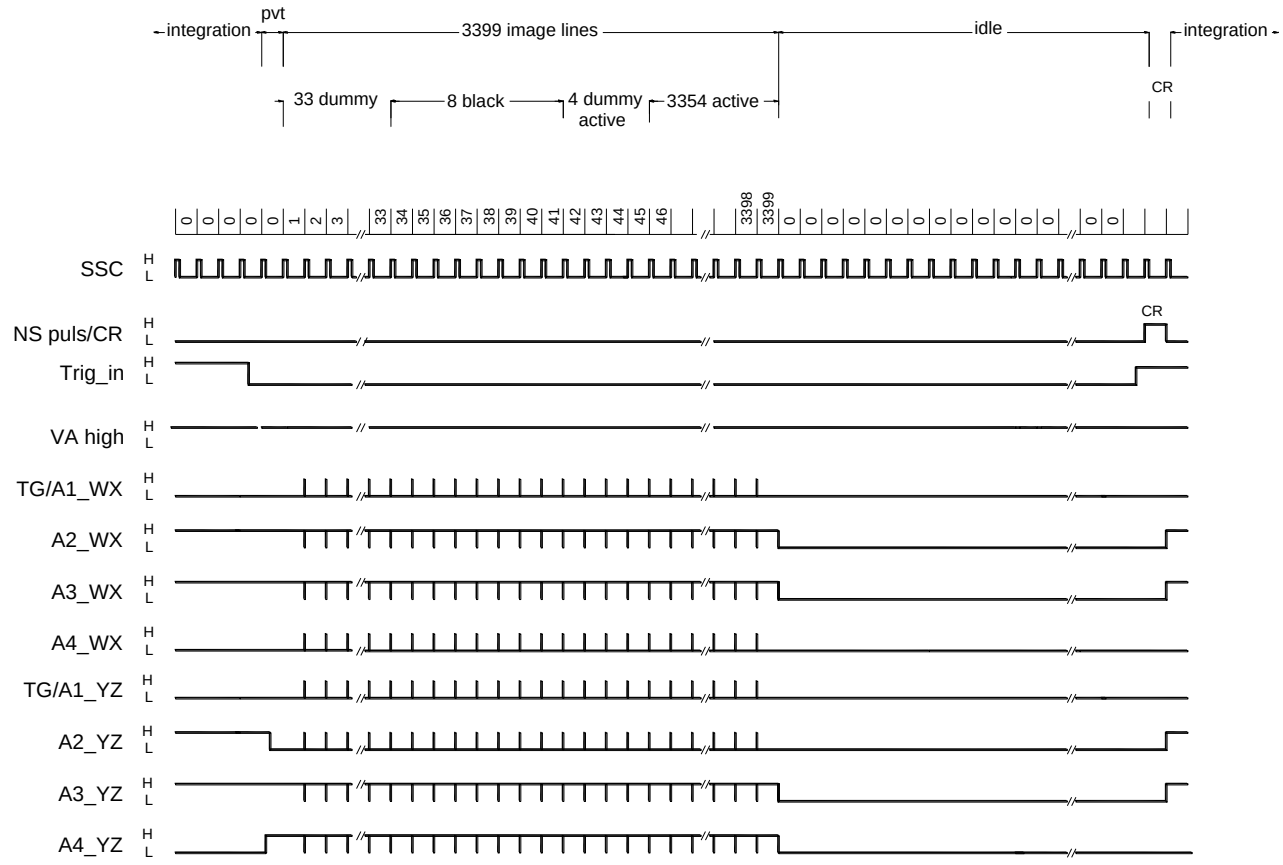

REMARKS
* CR is applied during the first line after the transition from L to H of Trig_in
* CCD is integrating during high period of Trig_in
* After readout sequence the timing will go into idle mode.
* Pvt means prepare for transport (only needed for readout through Y- and Z-output)

Figure 3: Frame Transport timing Diagram (Quad Output)

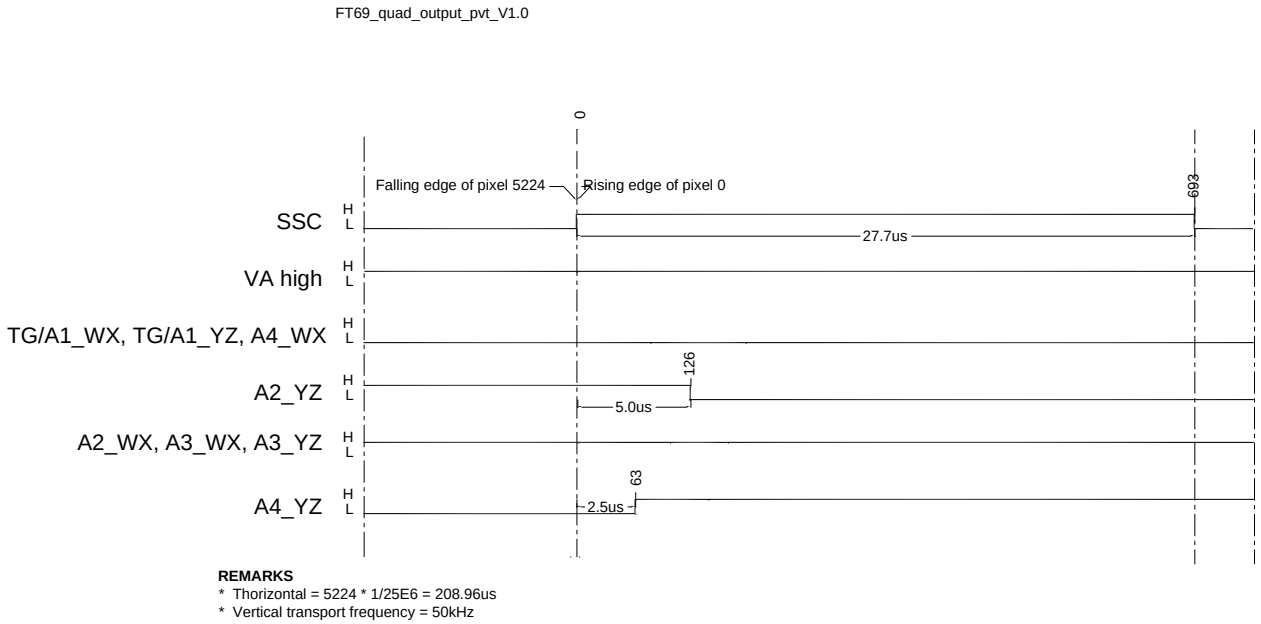

Figure 4: Prepare for Vertical Transport, Set A-Clocks for Split Vertical Readout

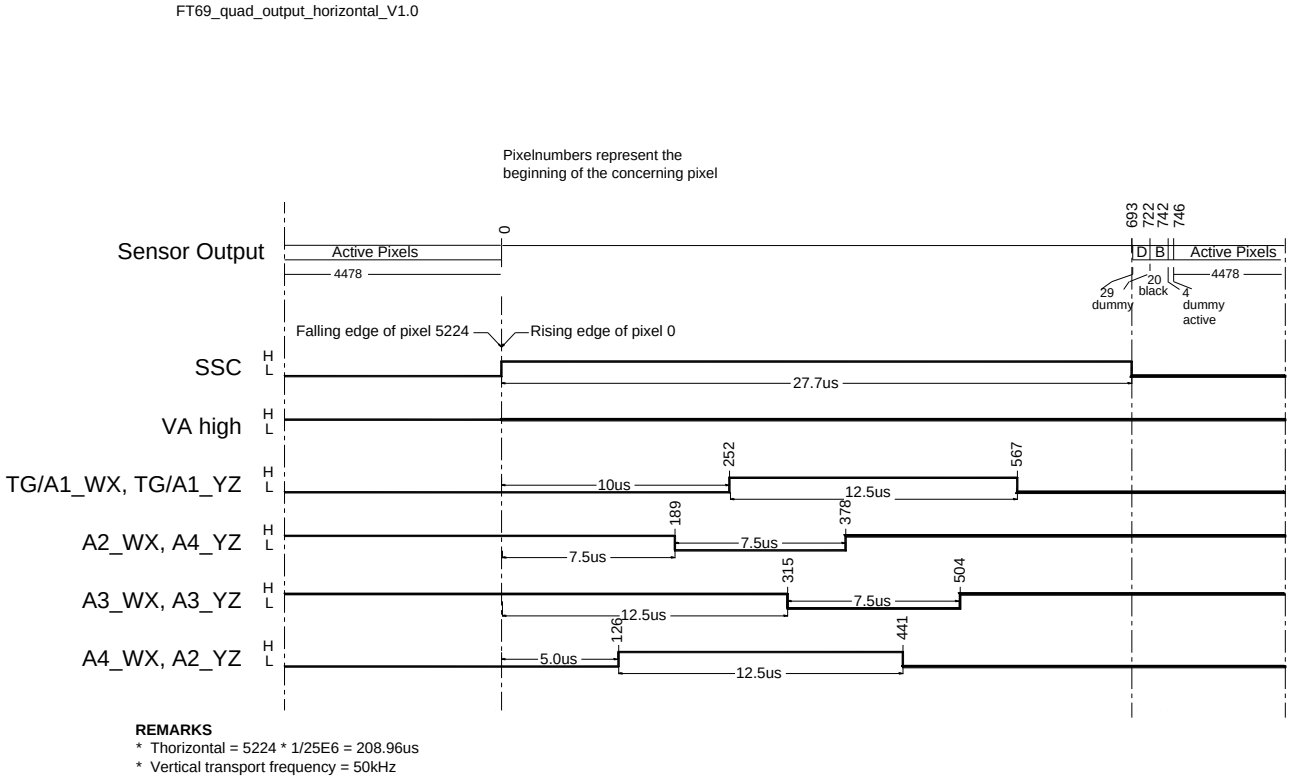

Figure 5: Timing Diagram Line Readout (Horizontal Split Dual Output)
For FMC, a similar transport concept is used

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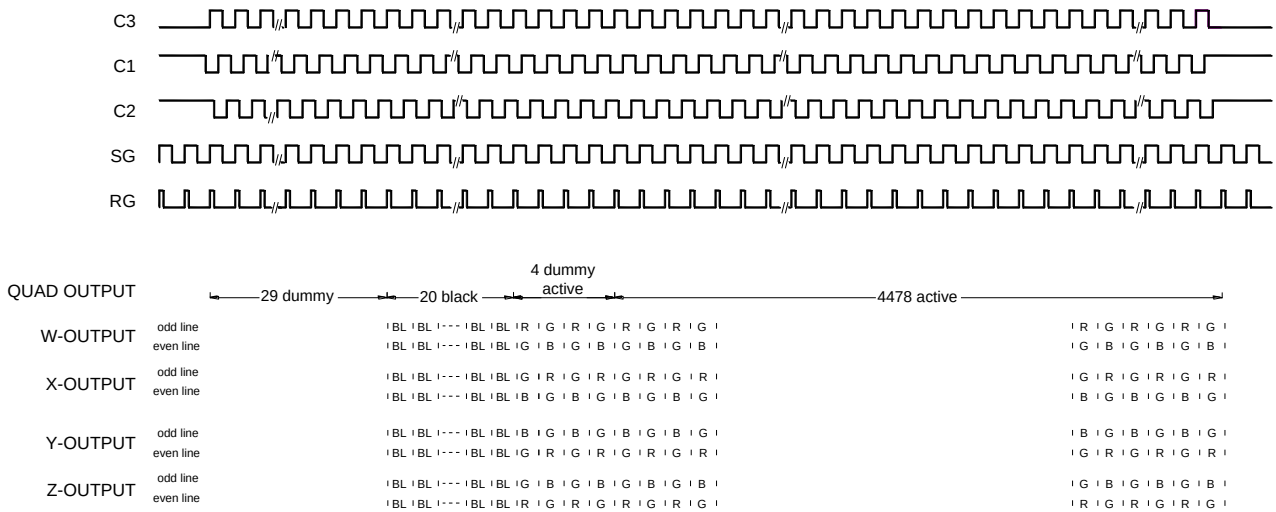

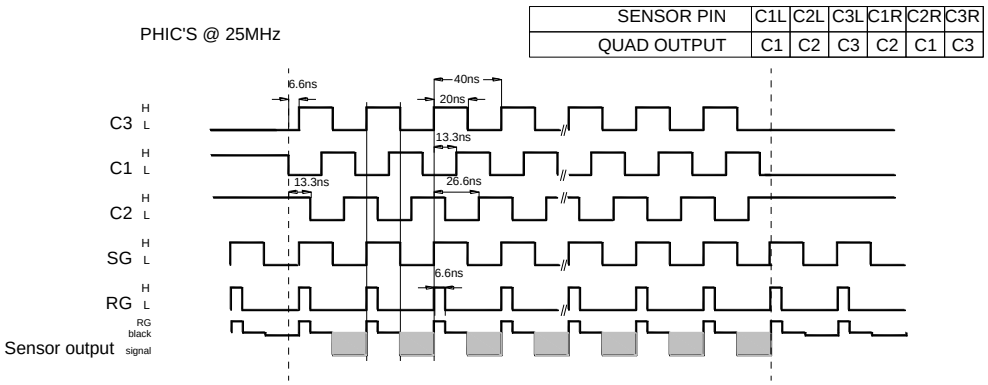

Figure 6: Horizontal Readout C-Clocks (Quad Output)

Performance

The test conditions for the performance characteristics are as follows:

- All values are measured using typical operating conditions.
- VNS is adjusted as low as possible while maintaining proper vertical anti-blooming
- Sensor temperature = 60°C (333K)
- Horizontal transport frequency = 25MHz
- Vertical transport frequency = 50kHz
- Integration time = 100ms
- Linear Operation, Linear/Saturation and Dark Condition parameters are measured at W, X, Y and Z outputs.

LINEAR OPERATION (W/X Output)	MIN	TYPICAL	MAX	UNIT
Charge Transfer Efficiency[1]	0.999995	0.999999	-	-
Image lag	-	0	0	%
Resolution (MTF) @ 83.3 lp/mm	60	-	-	%
Peak Quantum Efficiency in Blue @450nm		25		%
Peak Quantum Efficiency in Green @540nm		35		%
Peak Quantum Efficiency in Red @650nm		25		%
Peak Quantum Efficiency in near-Infrared @750nm		12		%
Block-to-block difference[2]		1.0	3.0	%
Stitching effect[3]		1.0	3.0	%
Low Pass Shading[4]		2	5	%
Random Non-Uniformity (RNU)[5]		1	2	%

[1] Charge Transfer Efficiency values are tested by evaluation and expressed as the value per gate transfer
[2] Block-to-block difference is defined as difference in average signal between different stitching blocks under illumination
[3] Stitching effect is defined as the deviation of response under illumination of the lines or rows at the stitch lines compared to the average response
[4] Low Pass Shading is defined as the ratio of the one-σ value of an 8x8 pixel blurred image (low-pass) to the mean signal value
[5] RNU is defined as the ratio of the one-σ value of the high-pass image to the mean signal of nominal light

OUTPUT BUFFERS	MIN	TYPICAL	MAX	UNIT
Conversion factor (ACF)	35	37	40	µV/el.
Mutual conversion factor mismatch (ΔACF)[1]	-	0	5	µV/el.
Supply current	-	5	-	mA
Bandwidth (R_{load}=3.3 kΩ)	100	120	-	MHz
Output impedance buffer (R_{load}=3.3 kΩ, C_{load}=2pF)	-	250	-	Ω
Amplifier noise over full bandwidth after CDS	-	11	13	el.

[1] Mismatching of the four outputs is specified as ΔACF with respect to reference W-output measured at the operating point (Q_{lin}/2)

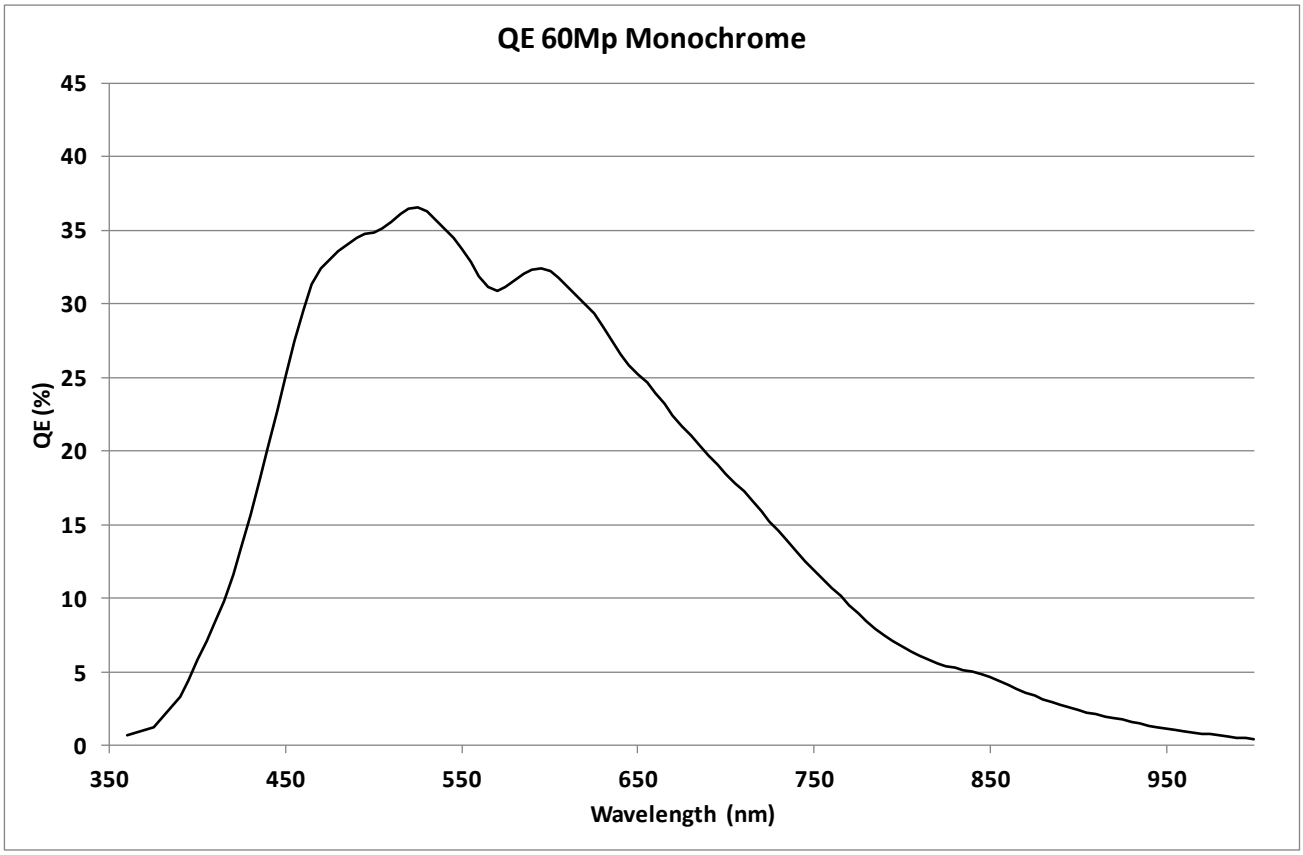

Figure 7: Typical Quantum Efficiency (QE) versus wavelength

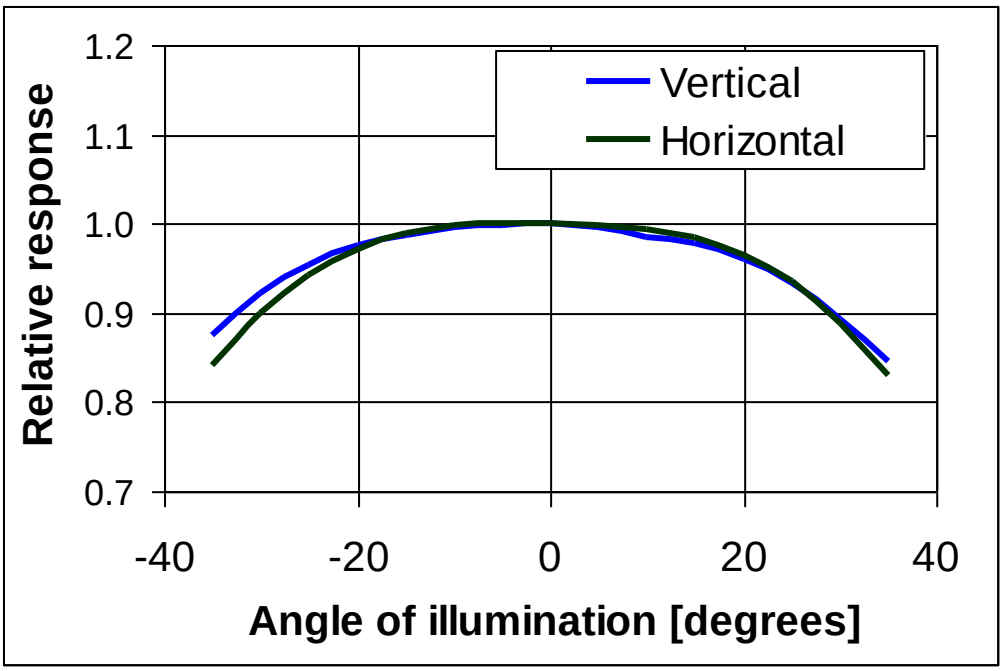

Figure 8: Angular response versus angle of illumination

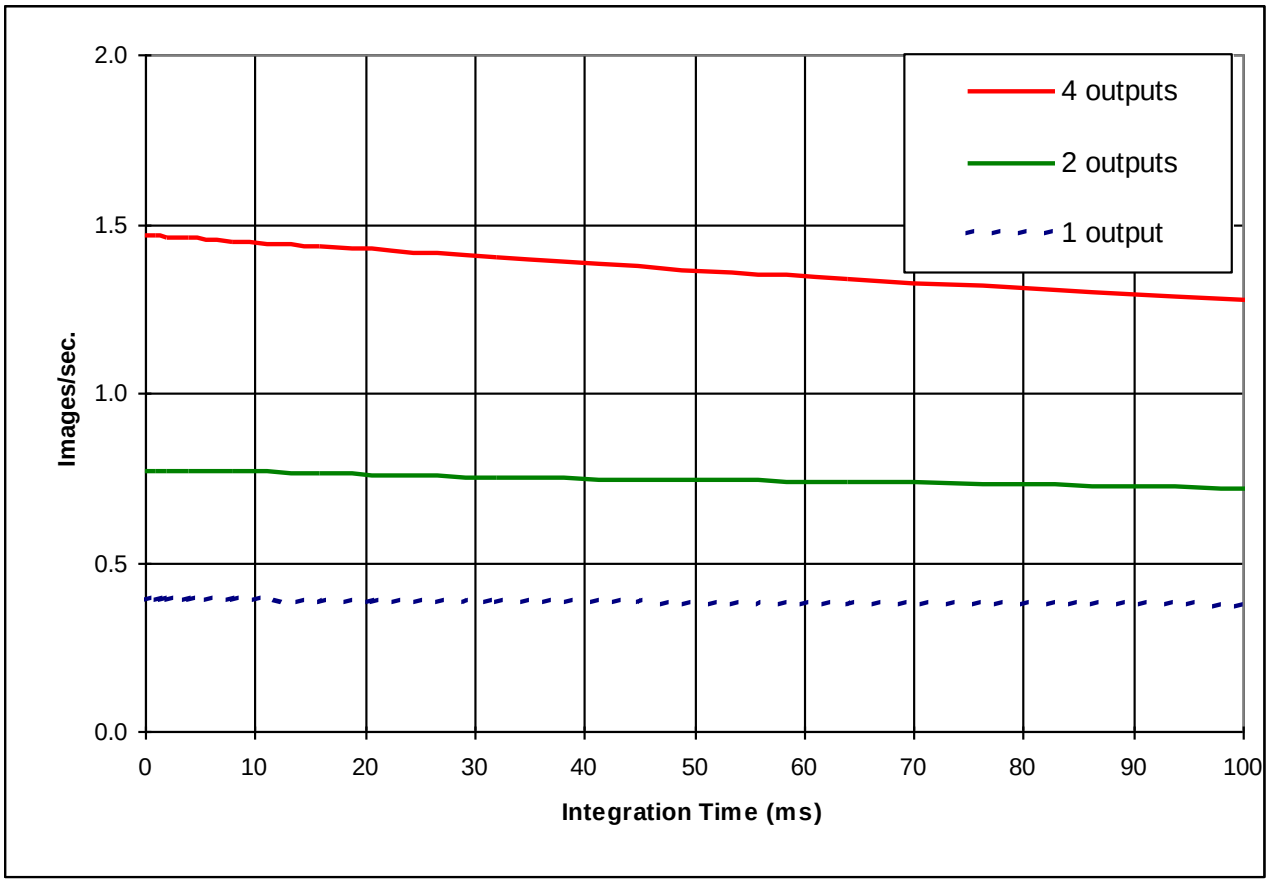

Figure 9: Maximum number of images/second versus integration time

LINEAR/SATURATION	MIN	TYPICAL	MAX	UNIT
Full-well capacity saturation level (Qmax)[1]	40000	50000	55000	el.
Full-well capacity linear operation (Qlin)[2]	30000	35000	-	el.
Overexposure[3] handling	-	200	-	x Qmax level
Dynamic Range	70	73	-	dB
Linear Dynamic Range	67	70	-	dB

[1]Qmax is determined from the low-pass filtered image
[2]The linear full-well capacity Qlin is calculated from linearity test (see dynamic range). The test guarantees 97% linearity.
[3]Overexposure over entire area while maintaining good Vertical Anti-Blooming (VAB) is tested by measuring the dark line along the image section.

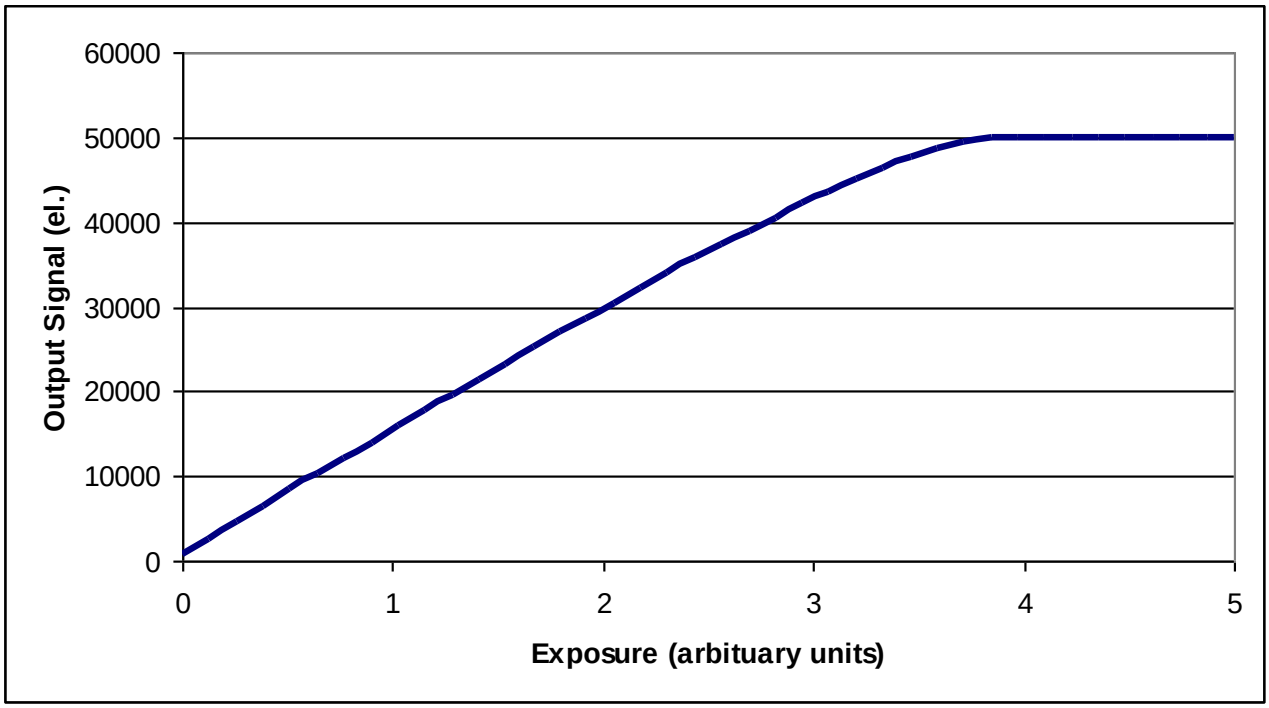

Figure 10: Charge handling

DARK CONDITION	MIN	TYPICAL	MAX	UNIT
Dark current level @ 20°C		3	7	pA/cm^2
Dark current level @ 40°C	-	16	35	pA/cm^2
Dark current level @ 60°C	-	100	200	pA/cm^2
Fixed Pattern Noise[1] (FPN) @ 60ºC	-	500	1000	el./s

[1]FPN is one-σ value of the high-pass image and normalized at 1 sec integration time

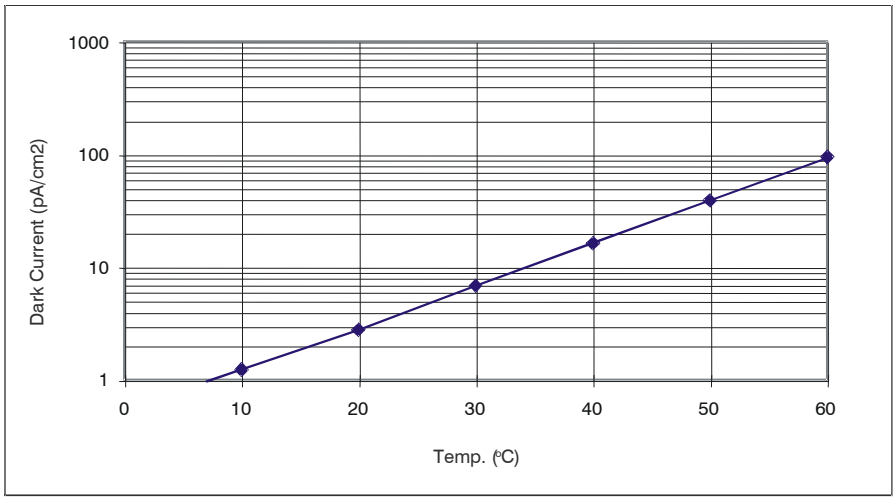

Figure 11: Dark current versus temperature.

Application information

Current handling
One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from overexposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure, a total current of 5 to 10mA through all VPS connections together may be expected. The pnp emitter follower in the circuit diagram (figure 12) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure, a total current of 5 to 10mA through all VNS connections together may be expected. The clamp circuit, consisting of the diode and electrolytic capacitor, enables the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Decoupling of DC voltages
All DC voltages (not VNS, which has additional CR pulses as described above) should be uncoupled with a 22nF uncoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current, which will float through VRD. Therefore, a large series resistor in the VRD connection may be used.

Image clocks
Though The image clock phases of quadrant W are internally connected to X, and the phases of Y are connected to Z, it is necessary to apply the driving voltages to all 4 quadrants (W, X, Y,Z).

Outputs
To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 250Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in the emitter follower; about 5mA should do the job. The collector of the emitter follower should be uncoupled properly to suppress the Miller effect from the base-collector capacitance.

A CCD output load resistor of 3.3kΩ typically results in a bandwidth of 120 MHz for X, W, Y and Z outputs.

Device protection
The output buffers of the FTF9168 are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 10mA. Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 12.

Color Imaging
The CCD is sensitive from 300nm up to 1100nm. This should be taken into account when using external colors filters. The cover glass is not an IR filter.

Unused sections
To reduce power consumption, the following steps can be taken. Connect unused output register pins (C1...C3, SG, OG) and unused SFS pins to zero Volts.

Device Handling

An image sensor is an MOS device, which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam, and in a dry and dark environment. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remains undamaged. When handling the sensor, use finger cots.

When cleaning the glass, we strongly recommend using ethanol. Use of other liquids is strongly discouraged:

- if the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches, which can destroy the device.

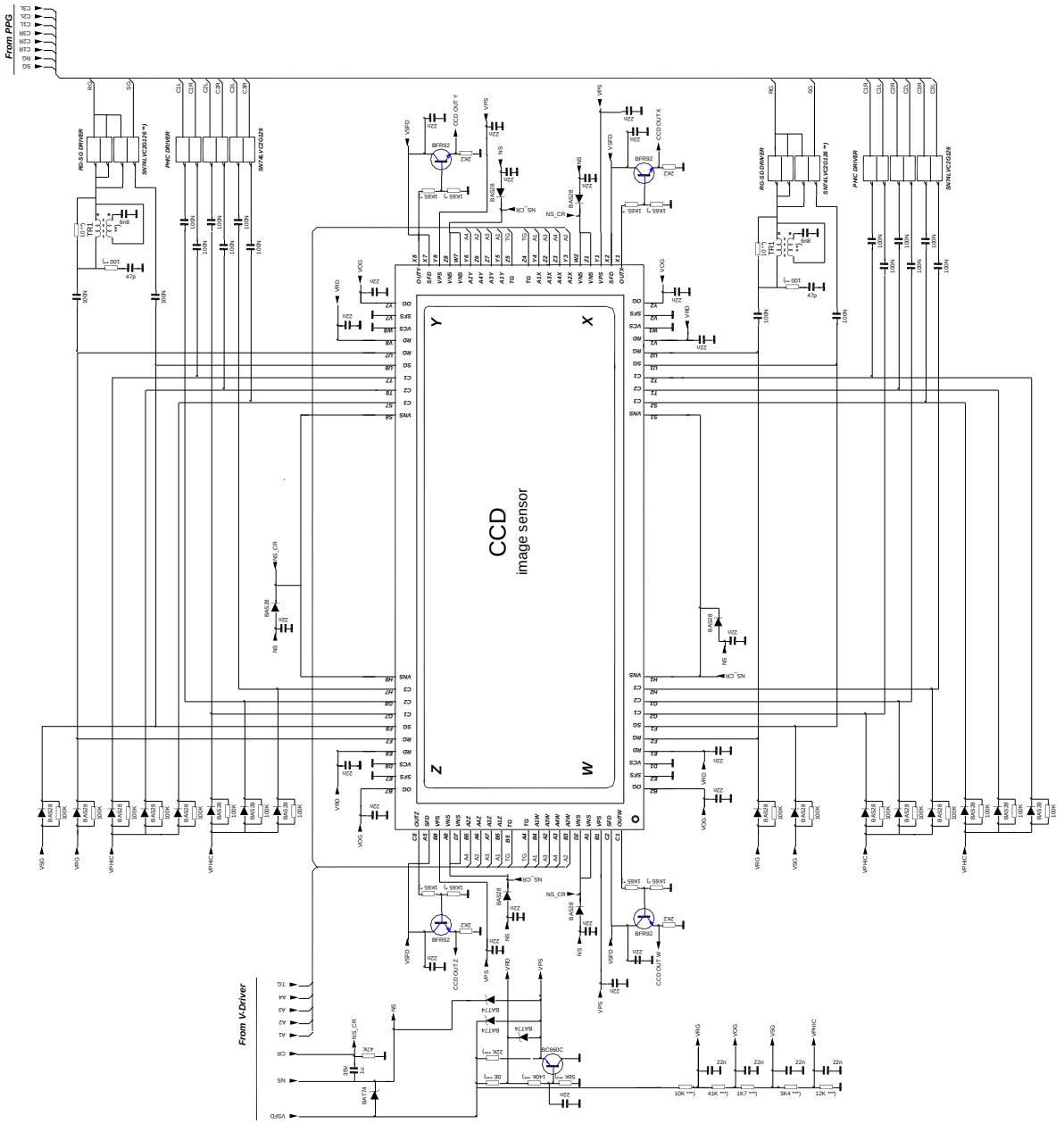

Figure 12: Application diagram

Pin configuration

The FTF9168 is mounted in a Pin Grid Array (PGA) package with 80 pins in a 20 x 25 grid of 53.44 x 67.23mm^2. The position of pin A1 (quadrant W) is marked with a gold dot on top of the package. The image clock phases of quadrant W are internally connected to X, and the phases of Y are connected to Z.

SYMBOL	Name	PIN # W	PIN # X	PIN # Y	PIN # Z
VNS	n substrate	A1	R1	R8	A8
TG	Transfer Gate	A4	R4	R5	A5
VNS	n substrate	D2	N2	N7	D7
VNS	n substrate	H1	J1	J8	H8
VPS	p well	B1	P1	P8	B8
SFD	Source Follower Drain	C2	O2	O7	C7
SFS	Source Follower Source	E2	M2	M7	E7
VCS	Current Source	D1	N1	N8	D8
OG	Output Gate	B2	P2	P7	B7
RD	Reset Drain	E1	M1	M8	E8
A1	Image Clock (Phase 1)	B4	P4	P5	B5
A2	Image Clock (Phase 2)	B3	P3	P6	B6
A3	Image Clock (Phase 3)	A2	R2	R7	A7
A4	Image Clock (Phase 4)	A3	R3	R6	A6
C1	Register Clock (Phase 1)	G2	K2	K7	G7
C2	Register Clock (Phase 2)	G1	K1	K8	G8
C3	Register Clock (Phase 3)	H2	J2	J7	H7
SG	Summing Gate	F1	L1	L8	F8
RG	Reset Gate	F2	L2	L7	F7
OUT	Output	C1	O1	O8	C8

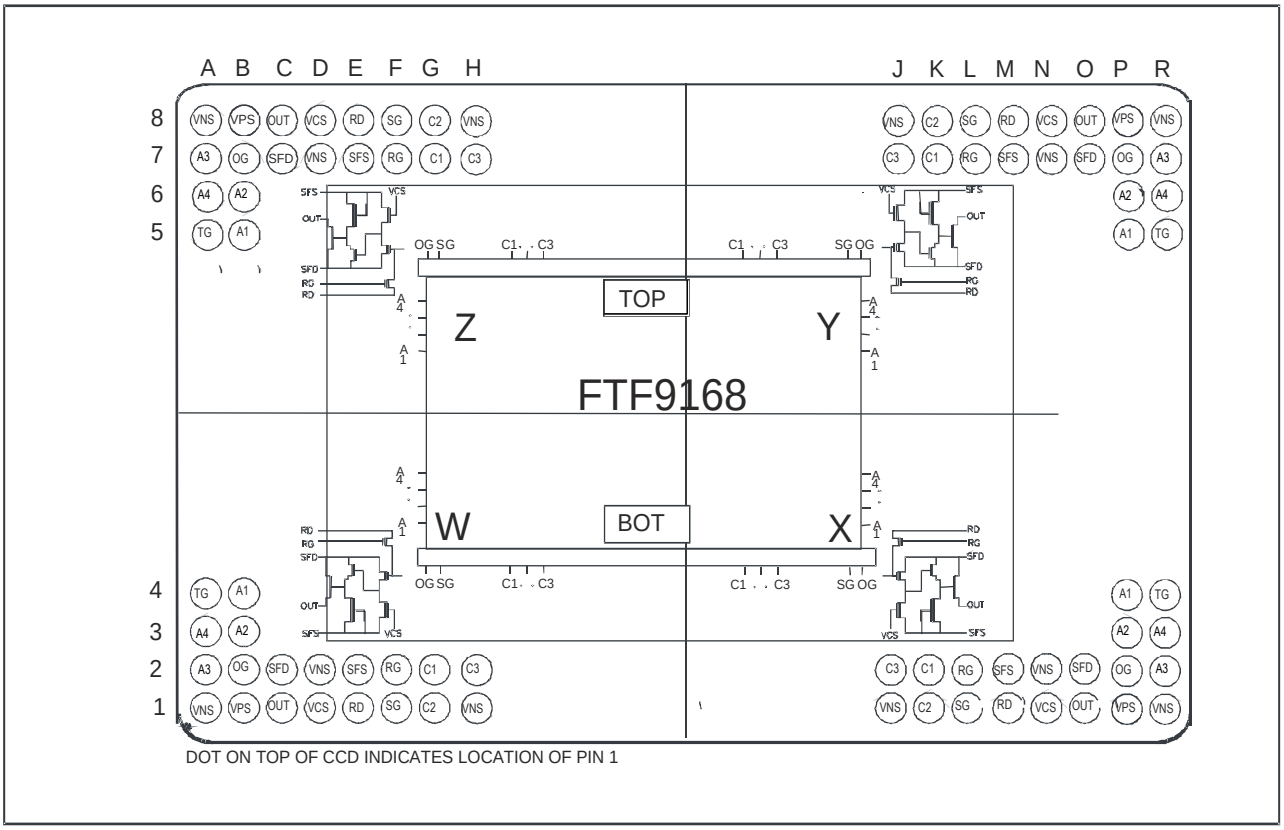

Figure 13: Pin configuration (Top view)

Package and coverglass information

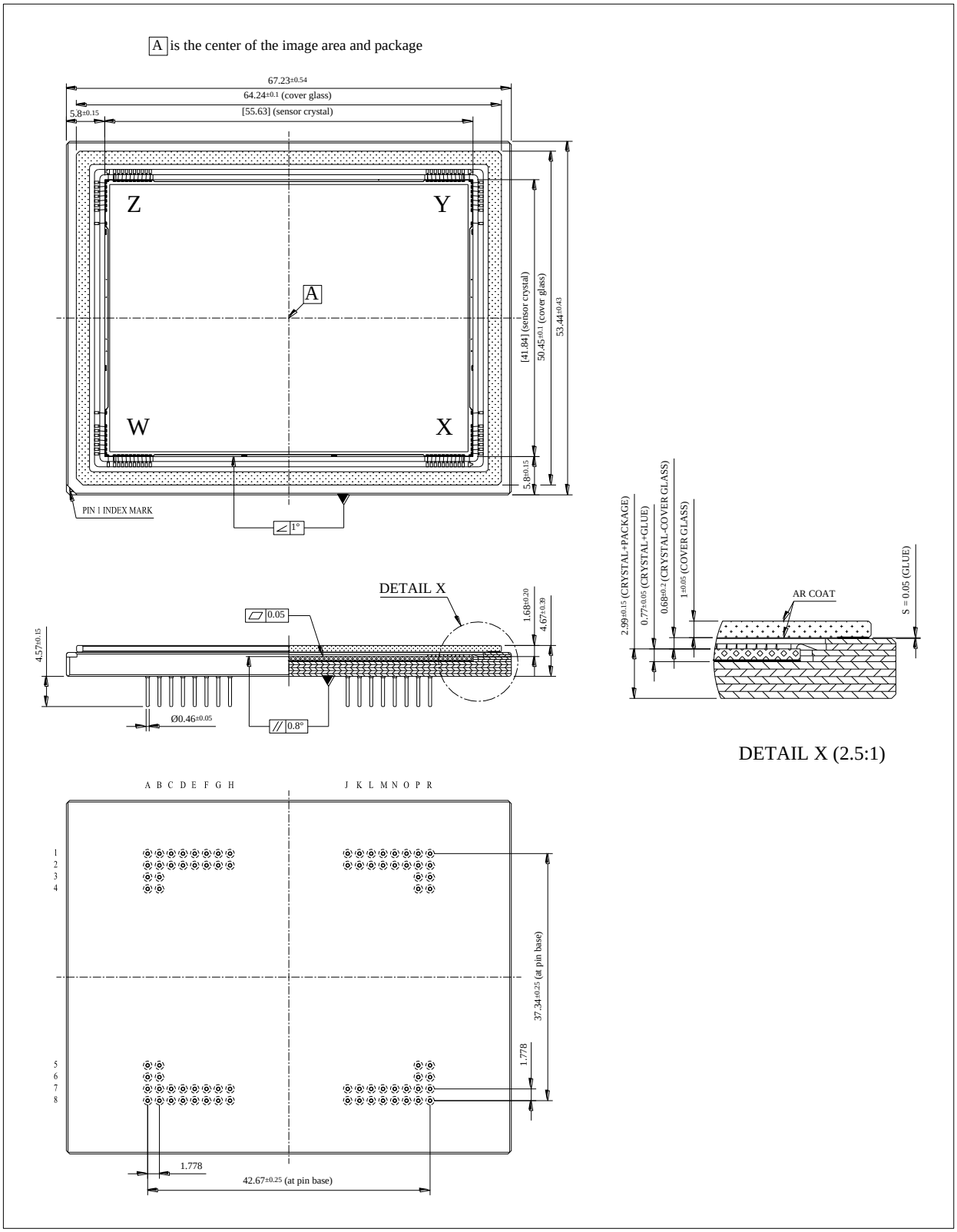

Figure 14: Mechanical drawing of the PGA package

Order Codes

The CCD image sensor can be ordered in a specific quality grade. The grading is defined with the maximum amount of pixel defects, column defects, row defects and cluster defects, in both illuminated and non-illuminated conditions. For detailed grading information, please contact your local Teledyne DALSA representative.

FTF9168C sensor		
Description	**Quality Grade**	**Order Code**
FTF9168M/TG	Test grade	9922-157-98132
FTF9168M/EG	Economy grade	9922-157-98152

For More Information
For more detailed information on this and other products, contact your local rep or visit our web site at http://www.teledynedalsa.com/sensors/products/products.asp

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This information is subject to change without notice.