AXIOM_LLSDADC1024fs

High Accuracy Low Latency ΣΔ ADC

Features

- Dynamic range: >114 dB (20 - 20kHz)
- Excellent THD performance:
  THD < -100 dBFS
- Integrated reference variants:
  a) low noise: >106dB SINAD
  b) high substrate rejection: 90dB SINAD
- Low out-of-band-noise (OOBN): -40 dBFS
- Robust against clock jitter
- Multi-bit advantages with a single bit modulator
- Full-scale differential input bandwidth: 60kHz
- VI conversion through user specific resistance
- Wide input common mode range
  - true ground
  - high voltage (>>V_{DDA})
- Power: 30mW per channel

Applications

- high-quality audio ADC & DAC (codec)
- fully digital closed loop amplifier
- high-precision control systems
- process and servo control
- active noise reduction systems

Description

The AXIOM_LLSDADC1024fs is a high-resolution sigma-delta analog-to-digital converter. The latency is only one effective data output period (40ns at f_{CLK}=50MHz), which makes the converter ideally suited for application in closed-loop digital control systems. The low latency is enabled by feedback of the bit stream output into a DAC with built-in filtering. This results in a “tracking ADC behavior”, where the output accurately tracks the input signal within the signal bandwidth. The filtering DAC makes the system robust against jitter and other error sources typically associated with 1-bit converters.

The AXIOM_LLSDADC1024fs is able to convert both single-ended and differential signals with high accuracy. The user specific VI conversion resistances enable a wide common and differential input voltage range, which could be well outside the supply level.

The information in this datasheet is preliminary and subject to change, awaiting results of the final test chip currently in processing.

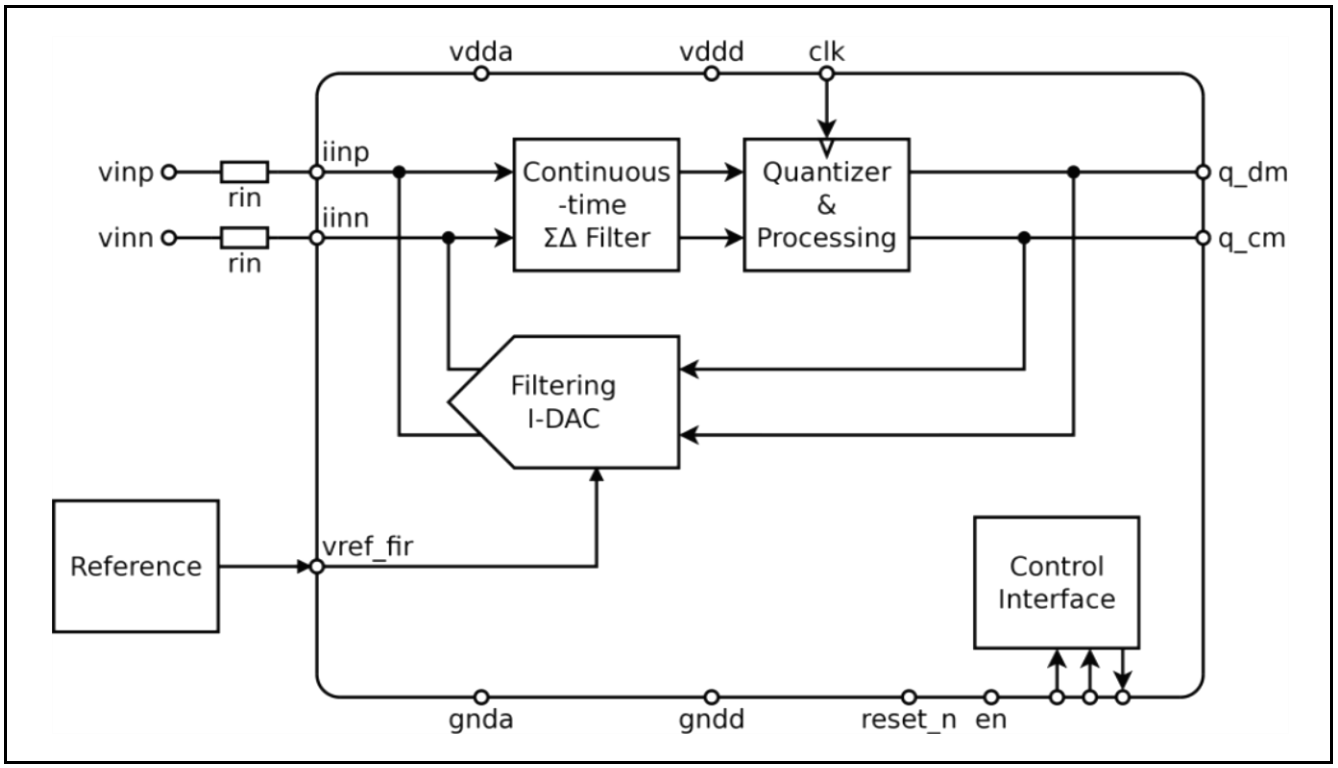

Figure 1 – Block diagram of the AXIOM_LLSDADC1024fs.

Specifications

Default test conditions

Digital supply voltage (V_{DDD})	1.8 V
Analog supply voltage (V_{DDA})	1.8 V
Temperature (T)	25 °C
Input clock frequency (f_{CLK})	45.1584 MHz (1024*44.1kHz)
Maximum analog input signal	25 Vp (0 dBFS), 2 x 5.1 kΩ Rin
Differential FIRDAC setting	7.5 mA
Common mode FIRDAC setting	9.2 mA
Used reference	axiom_c14_llsdadc1024fsrefgen

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
TECHNOLOGY					
NXP C14SOI	0.14µm CMOS SOI technology		0.14		µm
Area analog	Analog area		0.283		mm^2
Area digital	Approximated digital area		0.04		mm^2
Area refgen	Reference generator area		0.2		mm^2
TEMPERATURE					
T_{OP}	Operating temperature full performance	-40	25	150	ºC
T_{FO}	Functional operating temperature	-40	25	175	ºC
POWER SUPPLIES					
V_{DDA}	Analog supply voltage	1.65	1.8	2.0	V
V_{DDD}	Digital supply voltage	1.65	1.8	2.0	V
I_{DDD}	Digital supply current per ADC operating power-down[1]		 0.001	 2 0.005	mA
I_{DDA}	Analog supply current per ADC operating power-down		 0.001	 15 0.005	mA
$I_{DDA-REFGEN}$	Analog supply current reference gen operating power-down		 0.001	 4 0.005	mA
DIGITAL INTERFACING					
f_{CLK}	System clock frequency (1024fs)		45.1584	49.152	MHz
	Data output period		$f_{CLK}/2$		MHz
DC CHARACTERISTICS					
V_{REF}	Reference voltage used by the ADC[2]		0.9		V
V_{CM0}	Virtual ground voltage at input nodes[3]		0.9		V
I_{MAX-DM}	Differential input current for full-scale digital output q_dm[4]		7.5		mA_P
V_{OS-DM}	Differential input-equivalent offset (1σ)			5.0	mV
ΔG_{DM}	Absolute maximum differential mode DC voltage gain deviation[5]			3	%
ΔG_{CM}	Absolute maximum common mode DC voltage gain deviation[5]			3	%

[1] Power-down, clock off.
[2] Vref generated by axiom_c14_llsdadc1024fsrefgen.
[3] Input nodes iinn and iinp. The input signal common mode voltage (vinn and vinp) is uncorrelated to V_{CM0}.
[4] 7.5 mA is default for this test condition and corresponds to +3.8 dBFS input. Current is scalable through digital settings on axiom_c14_llsdadc1024fsrefgen.
[5] Gain deviation mainly determined by axiom_c14_llsdadc1024fsrefgen.

ΔG_{DM-REL}	Relative maximum differential mode DC voltage gain difference between ADC's sharing same reference[6]			0.35	%
ΔG_{CM-REL}	Relative maximum common mode DC voltage gain difference between ADC's sharing same reference[6]			0.35	%
AC CHARACTERISTICS					
DR_{DM}	Differential mode Dynamic Range[7]	114		120	dB
$SINAD_{DM}$	Differential mode Signal to Noise and Distortion ratio with default reference[8] 100Hz 1kHz 6kHz	 90 90 90			dB
$SINAD_{DM}$	Differential mode Signal to Noise and Distortion ratio with low noise reference[8] 100Hz 1kHz 6kHz	 106 106 106			dB
BO_{DM}	Differential mode back-off[9]		1.56		
BO_{CM}	Common mode back-off[10]		1.166		
Z_{IN-DM}	DC Differential mode input impedance[11]			0.1	Ohm
Z_{IN-CM}	DC Common mode input impedance[11]			0.5	Ohm
FS_{BW}	Full scale input bandwidth[12]		60		kHz
$I_{IN-DM-BO}$	Maximum differential mode input current while respecting the backoff[13] 1kHz 20kHz 100kHz >1MHz		 4.81 4.81 1.7 0.018		mA_P
$I_{IN-CM-BO}$	Maximum common mode input current while respecting the backoff @ 20 kHz[13] Sinking Sourcing		 -0.46 8.82		mA
SR_{DM}	Differential mode slew rate[11]			2.2	mA/µs
SR_{CM}	Common mode slew rate[14]			14	mA/µs
PSR	Power supply rejection[15] $\Delta V_{DDA} \rightarrow \Delta q\_dm$ $\Delta V_{DDD} \rightarrow \Delta q\_dm$ $\Delta V_{DDA} \rightarrow \Delta q\_cm$		 -80 -80 -40		dBFS
HWR	Handle Wafer rejection[16] $\Delta V_{HW} \rightarrow \Delta q\_dm$ @1kHz		-80		dBFS
CM2DM	Input equivalent common-mode to differential-mode conversion[17] $\Delta V_{DM}/\Delta V_{CM}$	-60			dB

[6] Assuming perfectly matched input conversion resistors
[7] Dynamic range definition: measure SNR @ -60 dBFS; DR = SNR+60 dB.
[8] Maximum ratio taken from top of SINAD vs Signal graph. Limited by modulated noise of the reference
[9] Margin required at input to maintain system performance. Results in full performance differential signal swing of -25 V to +25 V in default test condition (0dBFS). See Figure 2
[10] Margin required at input to maintain system performance. Results in 0 V to 17 V common-mode range in default test condition.
[11] Guaranteed by design
[12] The ADC however can convert higher input frequencies as long as the power of the input signal follows the envelope of the tracking transfer function, see $I_{IN-DM-BO}$.
[13] Required back-off is frequency dependent, this is equal to the envelope of the tracking adc. See for graphical representation, Figure 3.
[14] Common mode response spec useful for example in power supply modulated amplifiers (class DG/DH)
[15] Default power supply distortion: sine wave of 100 mV amplitude. Low noise reference used for measurement of differential mode power supply rejection. All numbers are based on an implementation without LDO.
[16] Handle wafer disturbance: sine wave of 100mV amplitude
[17] Input common mode test signal: 1kHz $1V_P$.

Table 1 – Specifications of AXIOM_LLSDADC1024fs

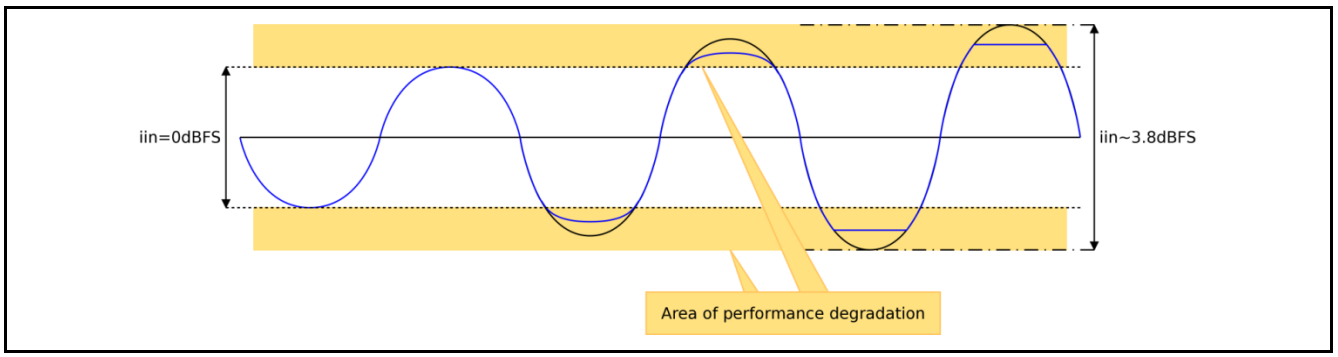

Figure 2 – Back-off margin to maintain system performance. Black input signal, blue converted signal

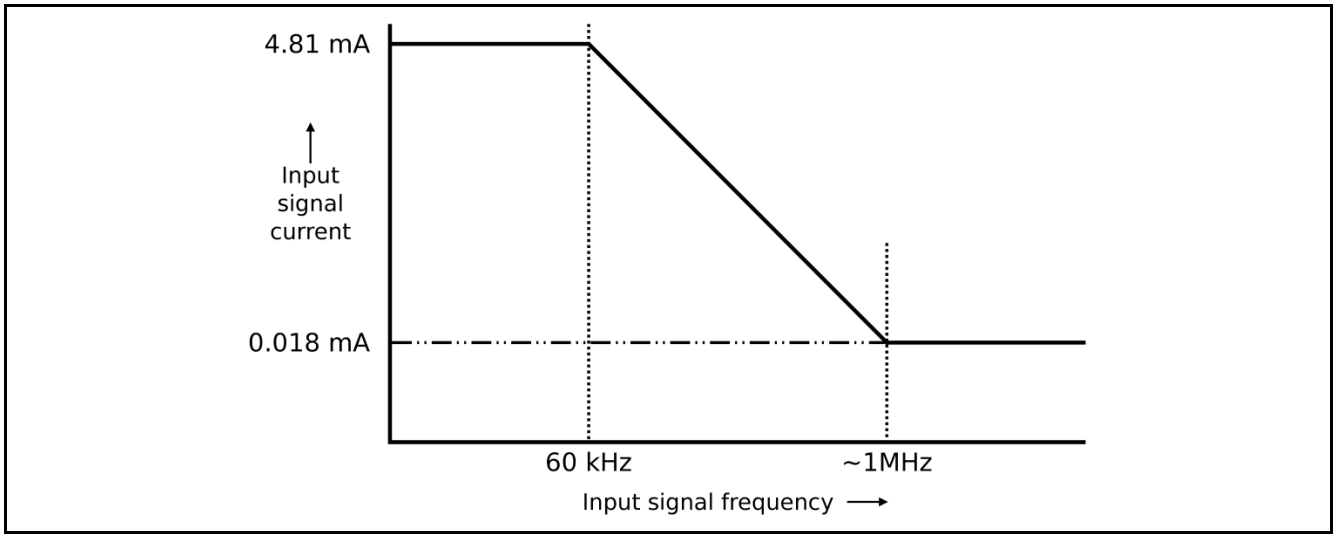

Figure 3 – Envelop of tracking ADC

Measured Performance

The following measurements are performed on the AXIOM_LLSDADC1024fs test silicon with encountered bugs. These bugs are well understood and solved in the next test silicon which is currently being processed. An update of the datasheet will be released with the validation results from the next silicon when available.
The current bugs increase the noise level, causes harmonic distortion like behavior and low amplitude idle tones.

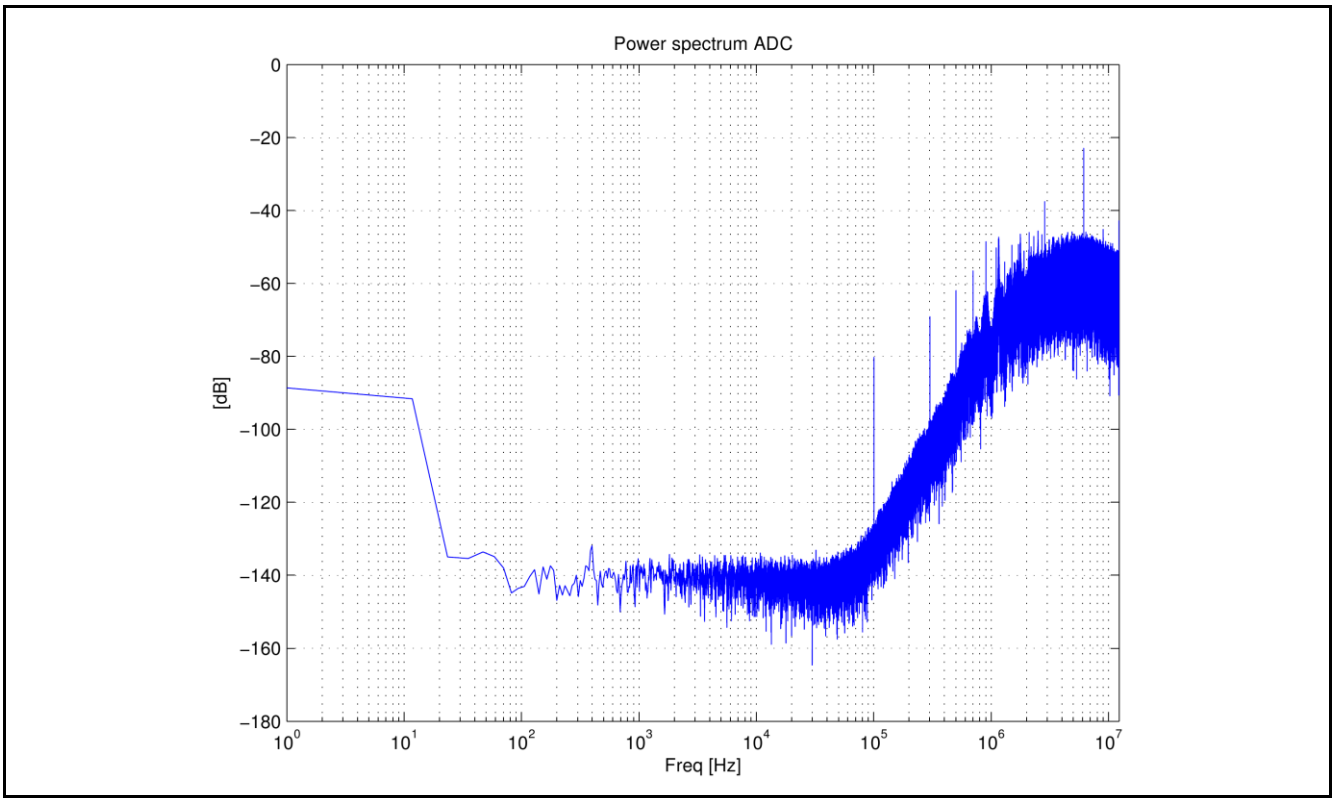

Figure 4 – Full spectrum of the AXIOM_LLSDADC1024fs no differential input

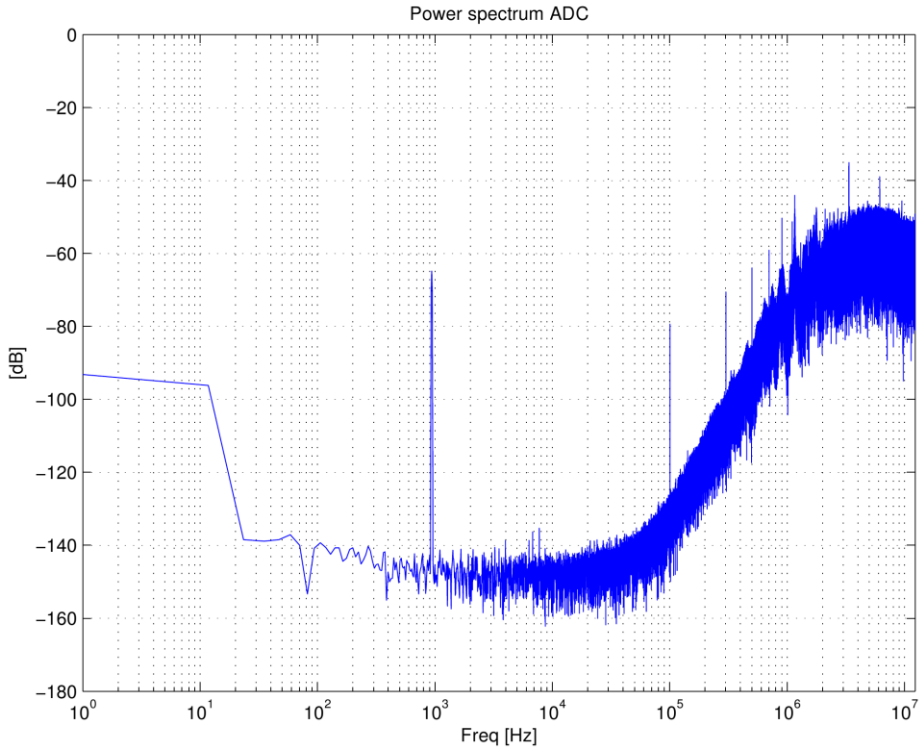

Figure 5 – Full spectrum of the AXIOM_LLSDADC1024fs with 25mVp input (-60dBFS). Minor tonal limit cycles are present in this spectrum, the updates will improve the tonal limit cycle suppression.

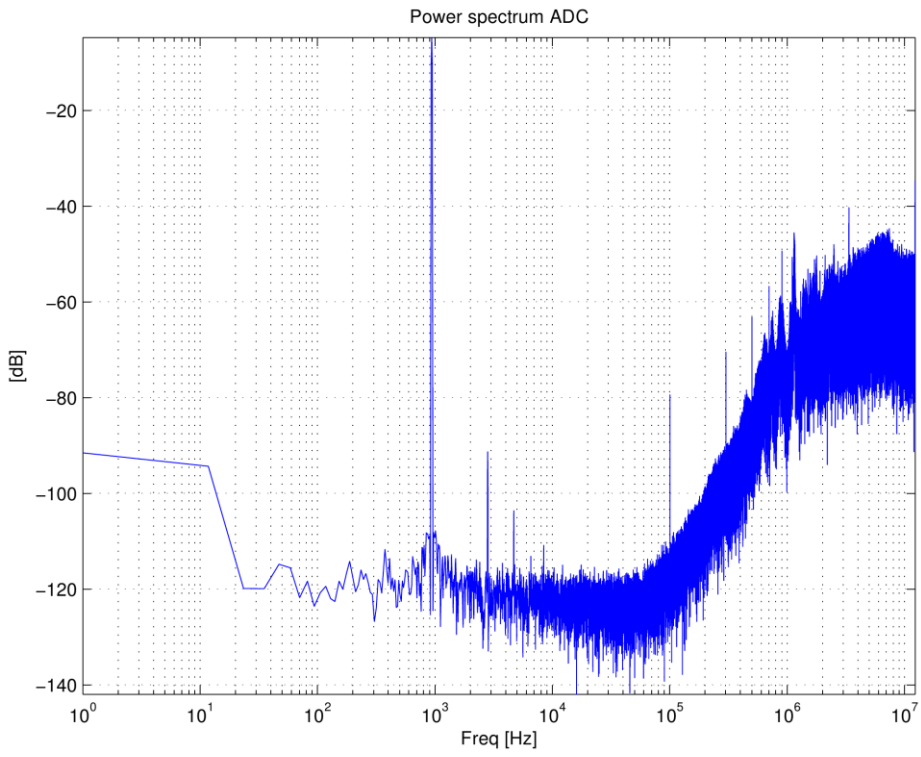

Figure 6 – Full spectrum of the AXIOM_LLSDADC1024fs with 25Vp input (0dBFS) The harmonic distortion visible in the above spectrum is caused by tracking tonal limit cycles. The updates on the next ADC suppress this behavior

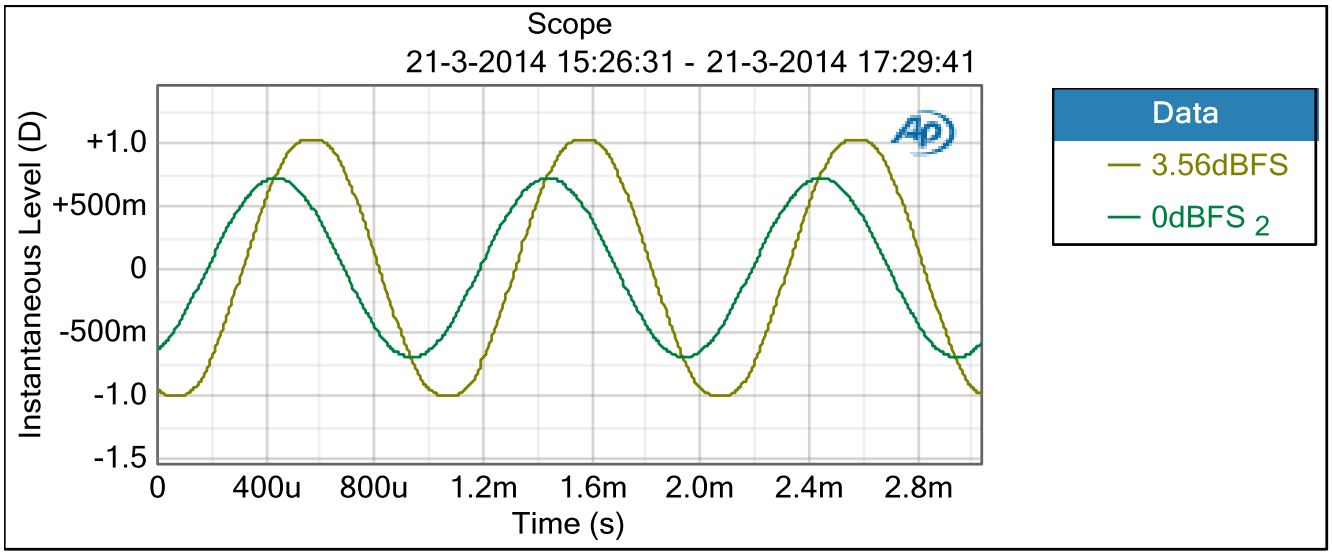

Figure 7 – 0dBFS vs 3.56dBFS input sine wave

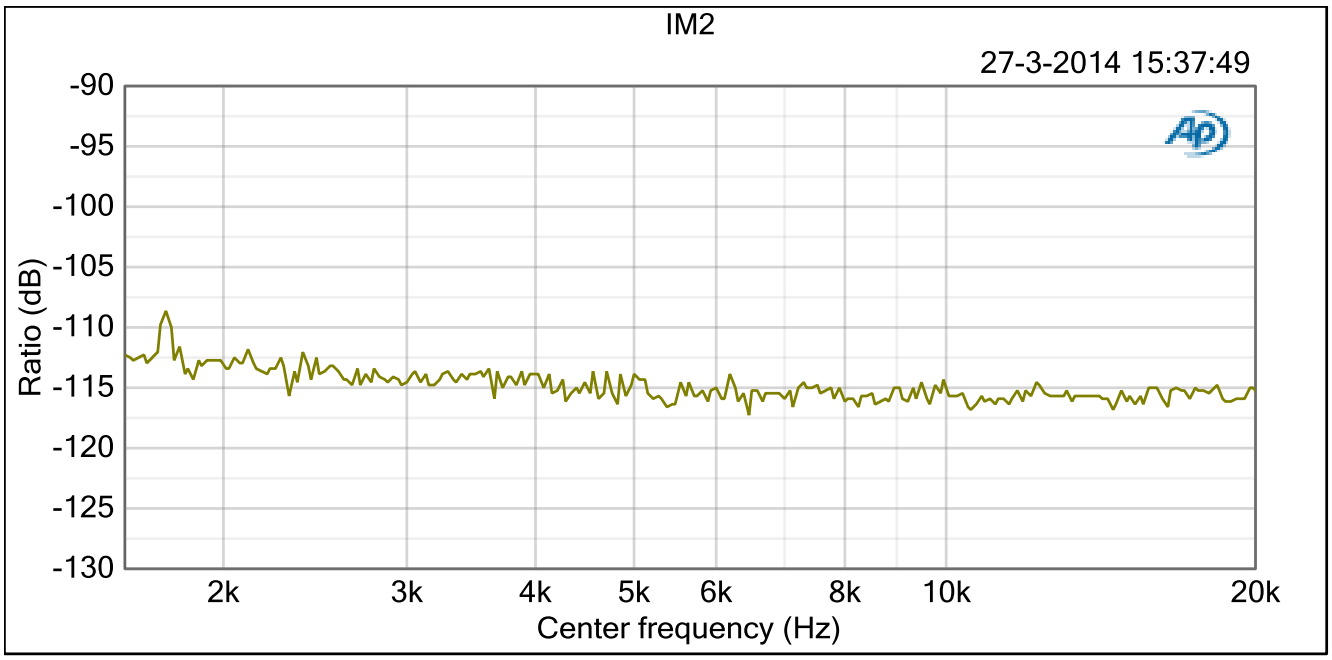

Figure 8 – IM2: sweep center frequency, 500Hz difference frequency. (both tones at -6dBFS)

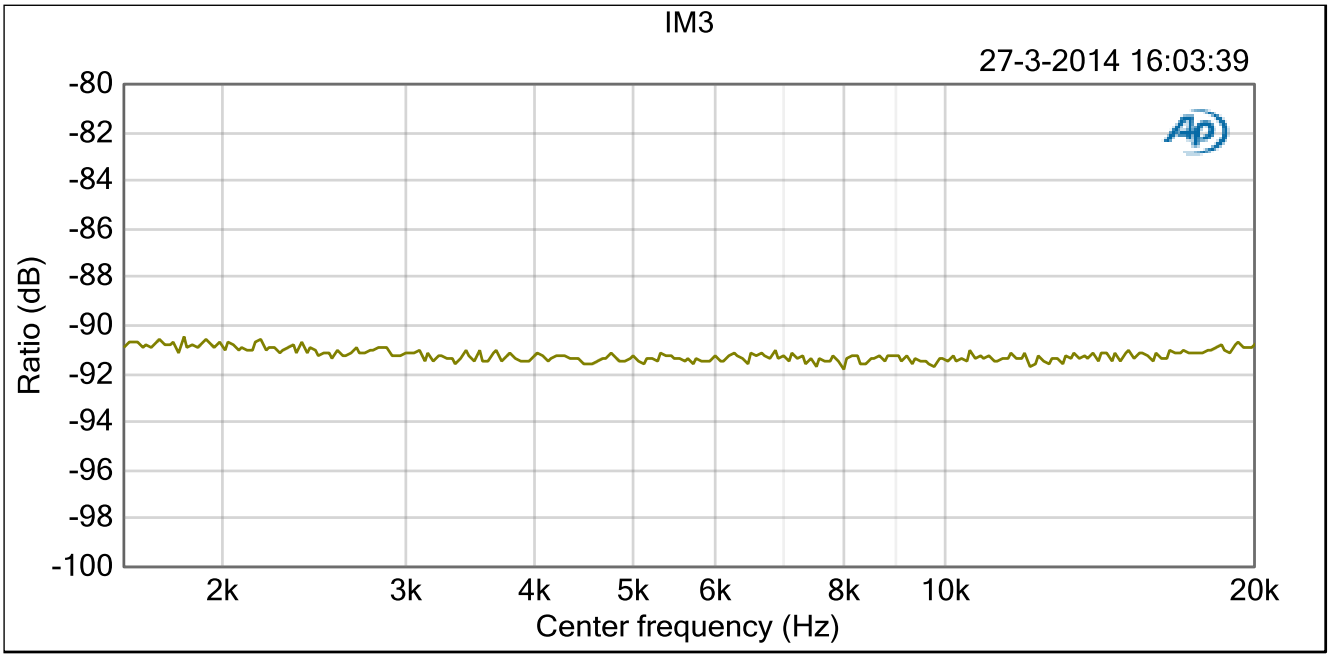

Figure 9 – IM3: sweep center frequency, 500Hz difference frequency. (both tones at -6dBFS)

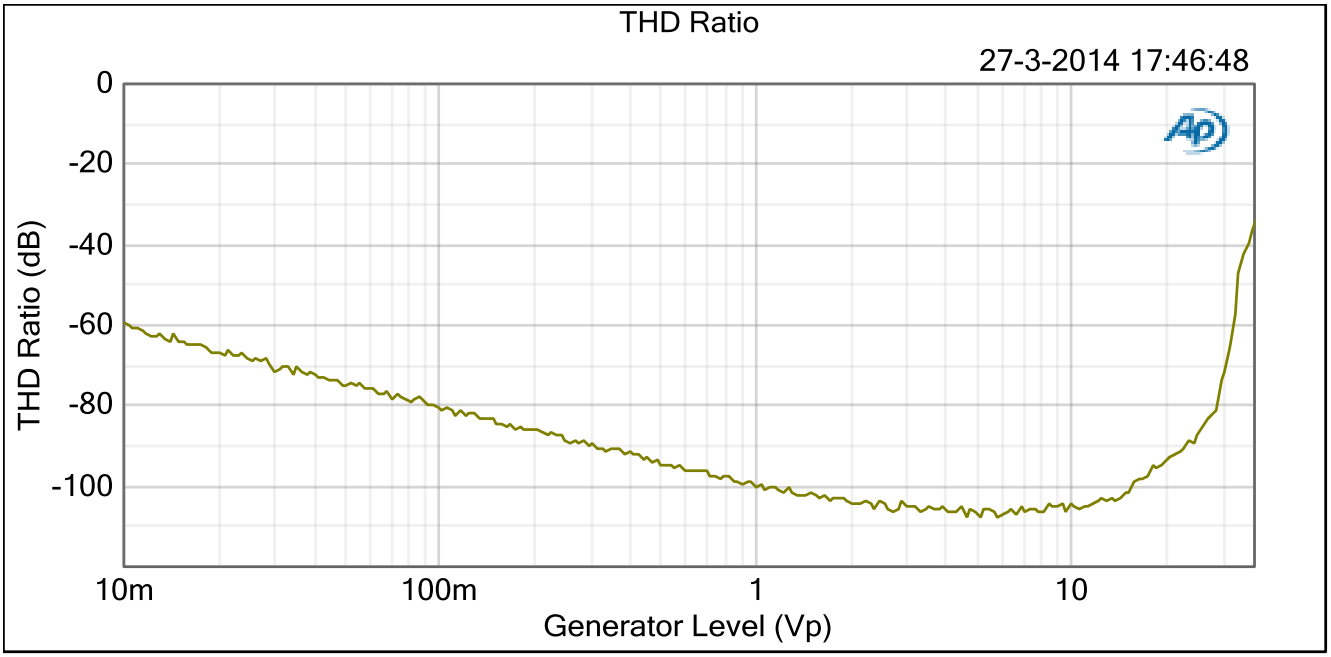

Figure 10 – THD ratio, sweep input amplitude 10mVp to 37.7Vp with 1kHz generator frequency

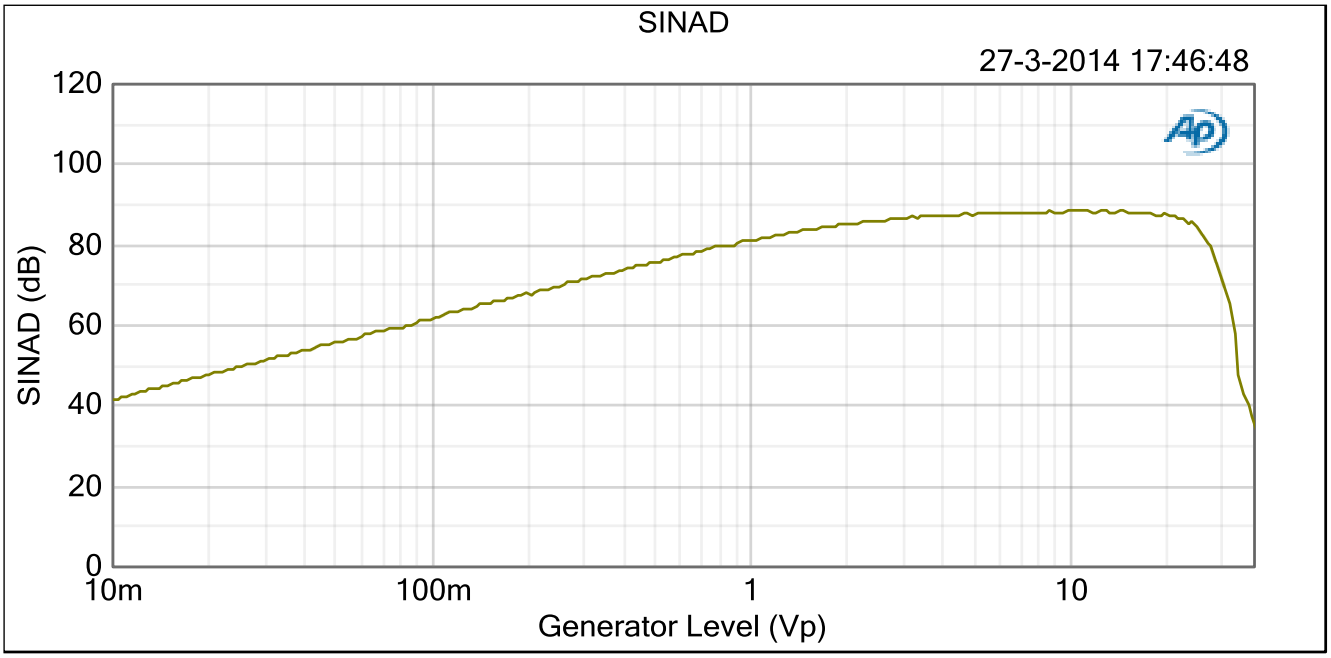

Figure 11 – SINAD, sweep input amplitude 10mVp to 37.7Vp with 1kHz generator frequency

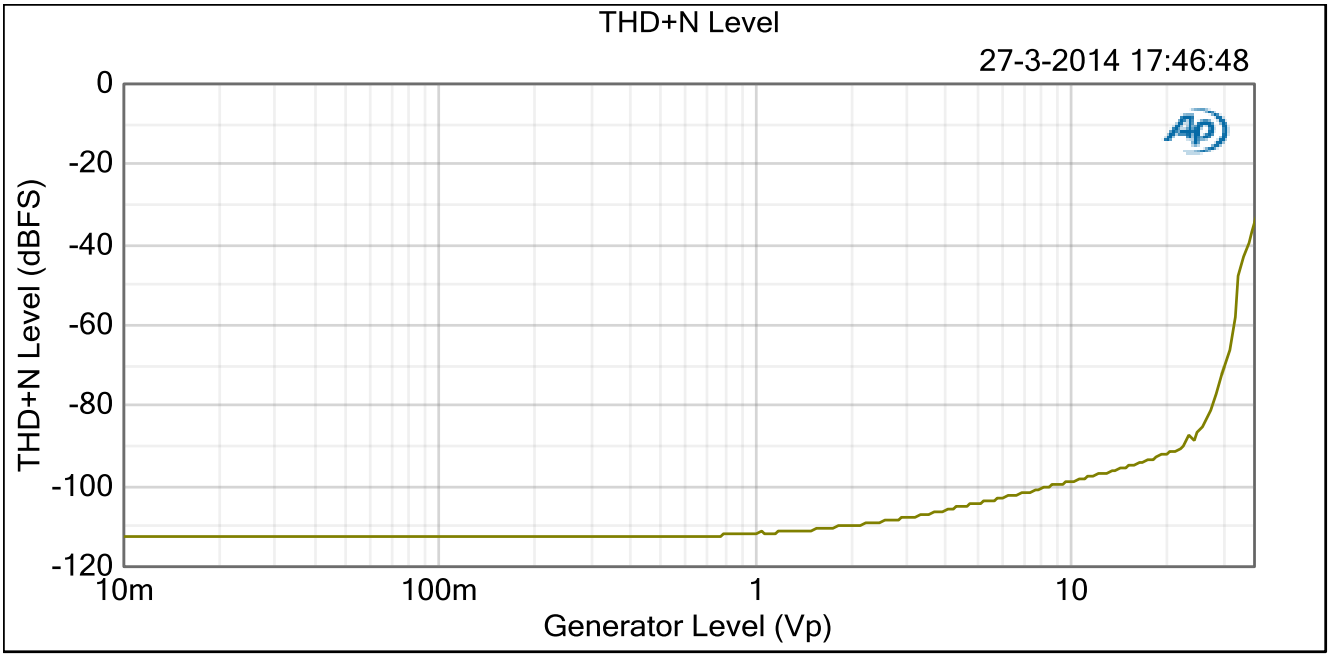

Figure 12 – THD+N level, sweep input amplitude 10mVp to 37.7Vp with 1kHz generator frequency

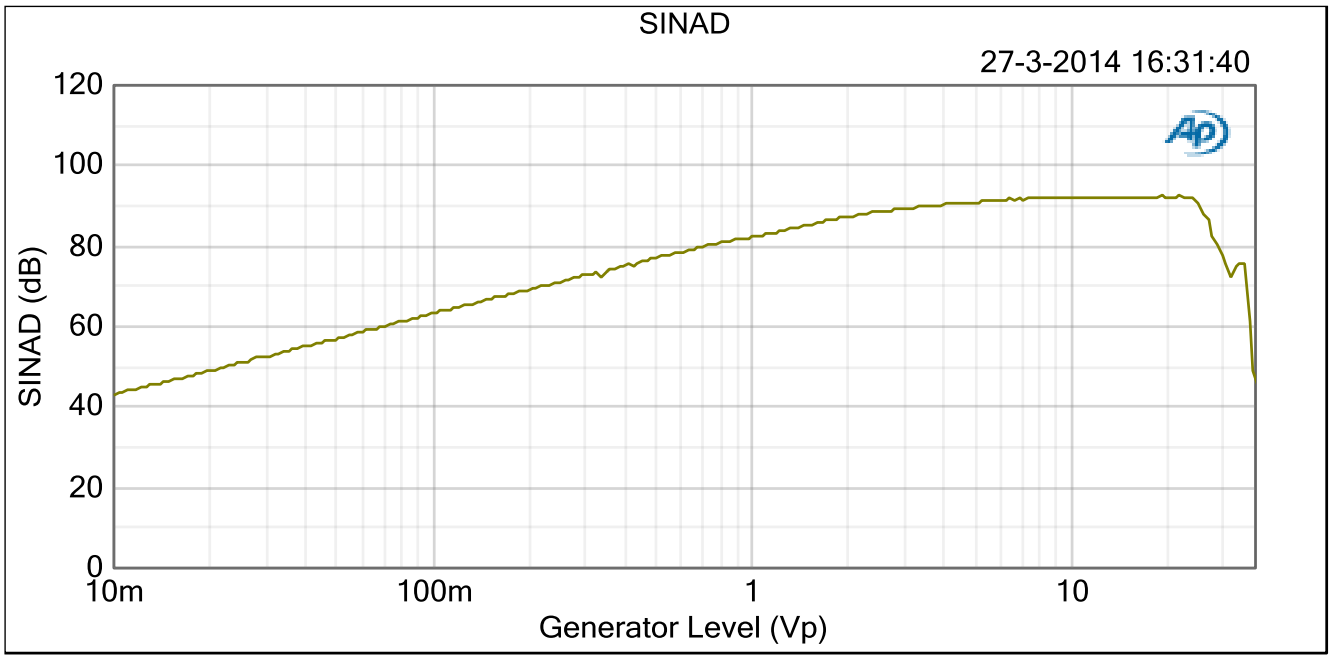

Figure 13 – SINAD, sweep input amplitude 10mVp to 37.7Vp with 20kHz generator frequency

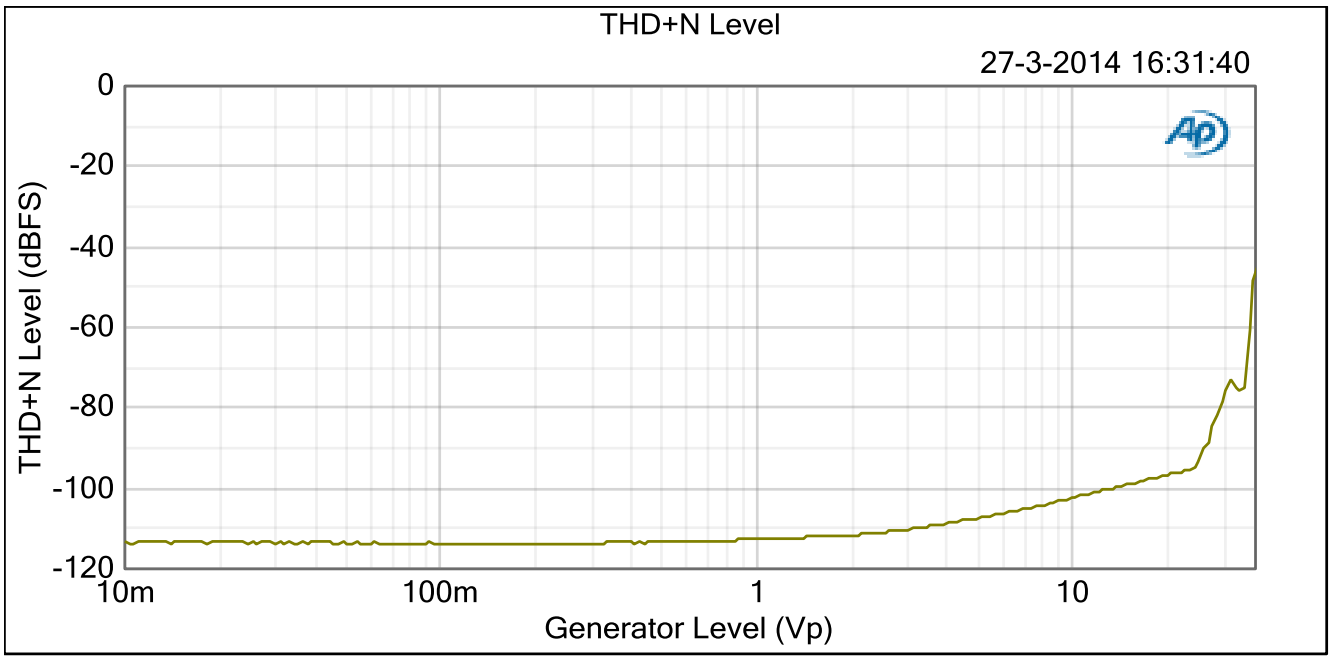

Figure 14 – THD+N level, sweep input amplitude 10mVp to 37.7Vp with 20kHz generator frequency

The 20kHz measurements give good insight in harmonic distortion behavior of the ADC. If compared to the 1kHz sweep measurements the noise level mainly determines the performance. Harmonic distortion is currently limiting the performance at higher input amplitudes >0dBFS, but will be solved in the next version of the ADC.

Applications

The AXIOM_LLSDADC1024fs is versatile and can be used in many applications; examples of applications are given in the following sections.

Digital amplifier

Enabled by its low latency, the AXIOM_LLSDADC1024fs can be integrated in a truly digital amplifier. Figure 15 shows for example the embedding of the AXIOM_LLSDADC1024fs in a Class-D amplifier with feedback after the LC-filter. The key advantages of a truly digital amplifier are: improved performance due to digital loop design, fast design cycles and reduces costs.
For more information on digital amplifiers see our website: http://www.teledynedalsa.com/semi/mixed-signal/HRLLSDADC/
(under the applications tab you can find a presentation on the digital amplifier concept)

Instrumentation

The AXIOM_LLSDADC1024fs can be used to make precision measurements for a wide range of input configurations. Figure 16 shows three input configurations; fully differential, single-ended and true ground. Both the differential and the common-mode signals are converted into a bit stream and available at the output.
The ADC can convert signals well outside its supply range enabled by the input conversion resistance. This resistance can be tailored to a specific input voltage range (differential-mode and common-mode).

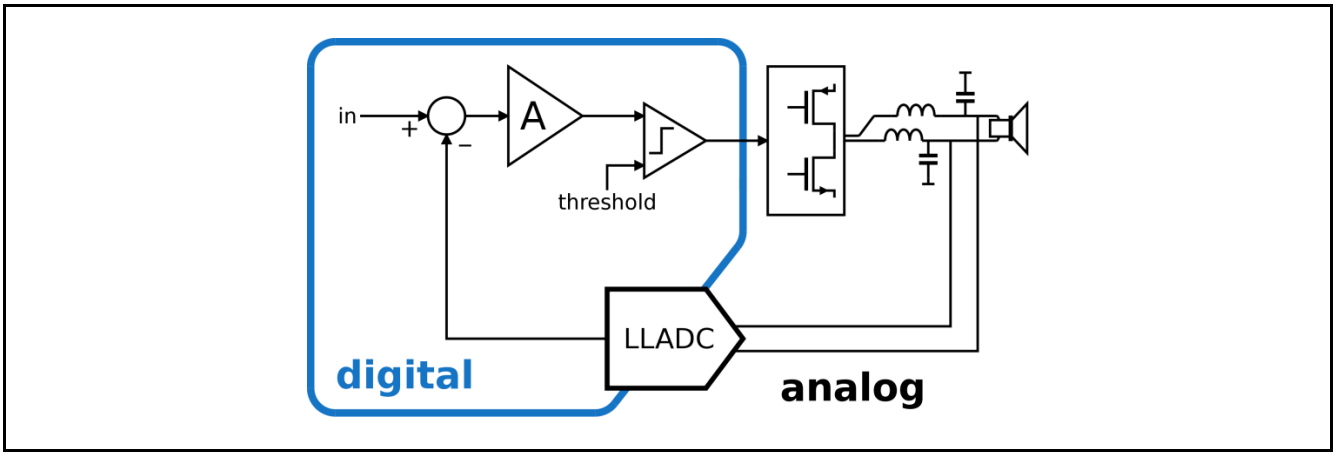

Figure 15 – Block diagram of the AXIOM_LLSDADC1024fs in a digital amplifier.

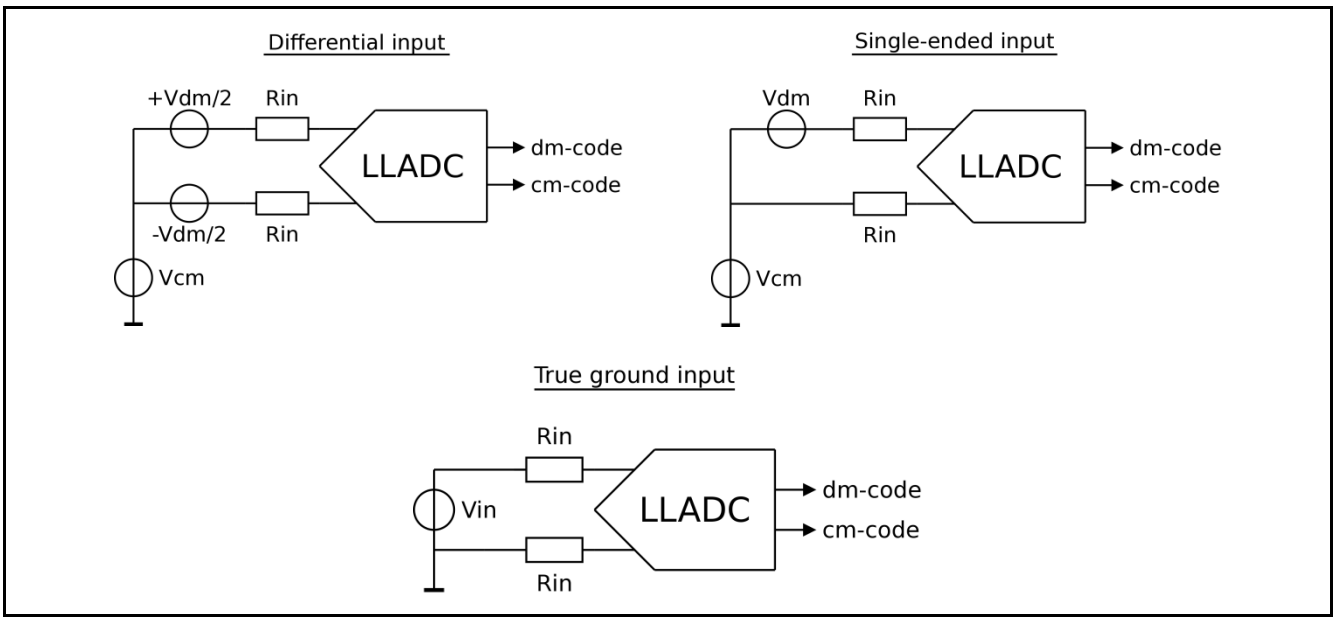

Figure 16 – Input configurations of the AXIOM_LLSDADC1024fs for precision instrumentation measurements.

Digital noise cancellation

The AXIOM_LLSDADC1024fs is well suited to digitize the output of a microphone. The latency of the AXIOM_LLSDADC1024fs (~40ns) is more than 1000 times lower than the period of a 20kHz signal (50us). This unique property of the AXIOM_LLSDADC1024fs enables digital noise cancellation with feedback, using adaptive noise suppression algorithms. The application diagram is shown in Figure 17. The digital noise cancellation core combines the unwanted noise signal (sensed via mic) with the wanted signal (in) such that at the output the unwanted signal is suppressed at the speaker/headphone.
At our website an alternative can be found when less power is required:
http://www.teledynedalsa.com/semi/mixed-signal/LLSDADC100dB/

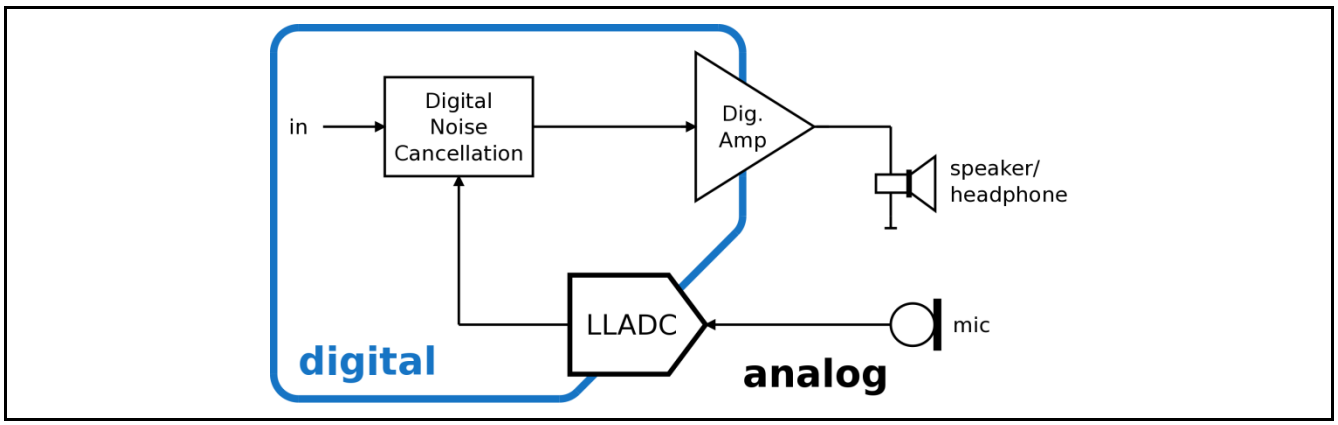

Figure 17 – Application of the AXIOM_LLSDADC1024fs (“LLADC”) for digital noise cancellation.

Delivery

The IP deliverables consist of a GDS file, a behavioral model, a netlist, a datasheet and integration documentation. The product can be delivered as a single IP component for customer integration or Teledyne DALSA engineers can integrate the product as part of a SoC engagement.

VIEW	FILE TYPE	DESCRIPTION
Behavioral model	VHDL / Verilog / Simulink	Behavioral model of the IP which can be used for simulation purposes
Netlist	CDL	Netlist for LVS checks
Layout	GDS2	Layout database
Abstract	LEF	Abstract view with layout boundaries and pinning information
Checks	DRC/LVS/ANT	Verification checks results performed on the layout
RTL	VHDL	VHDL code
Timing & interface	SDC & LIB	Timing constrains and interface information
Design documentation	PDF	Datasheet, specifications and simulation results
Integration documentation	PDF	Interface description for integration

Table 2 – Deliverables of the IP

Revision history

REVISON	DATE	REASON FOR REVISION
D2a		Initial version, copied from old template datasheet
D2c/d/e/f/g	2014-03-13	Updated template styles, header, table/figures
F2		Release for publication on the website
F3	2014-04-02	Updated Zin, slewrate, PSR and HWR specification text

Table 3 – Document revision history

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

or contact us at

Teledyne DALSA
Colosseum 28
7521 PT Enschede
+31 (0)53-7370010
info.enschede@teledynedalsa.com