# High Voltage Charge Pump Using Standard CMOS Technology

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***Abstract*-An integrated high voltage charge pump circuit utilising intrinsic process features is introduced. It can produce +20V to +50V output from a typical 5V input. The reported charge pumps achieved the highest density and highest output voltages of the industry. Measurements show output ripples of 400mV for frequencies around 10MHz and output load of 28pF. The reported integrated high voltage charge pump circuits was implemented on 0.8µm DALSA Semiconductor technology using standard CMOS devices.**

## I. INTRODUCTION

Demand for lower supply voltage is getting stronger as portable applications become more popular. Since many processes are not specified for voltages above 5V, requirements for higher power supply voltage and ability to deal with such voltages can become challenging with today's applications. This is particularly true for automotive parts, telecom interfaces, cellular phones and microelectromechanical systems (MEMS), which often require high supply voltages.

The operating supply voltage for high voltage (HV) applications is increasing steadily, ranging from 20V to 300V. Most commercially available and reported charge pumps are limited to maximum output voltages between 12V and 15V. To achieve higher output voltages, bulky, slow and costly solutions based on external discrete components tend to be used.

This paper demonstrates that integrated charge pump circuits can be used to boost a standard low input supply voltage to produce +20V to +50V output voltage. These charge pumps offer excellent performance. For instance, the circuits discussed in this paper have some of the highest voltage gain reported [5]. The proposed solution exploits unique process features in order to achieve the highest density and highest output voltages of the industry [1]. Several papers report integrated charge pumps [2], [3] and [4]. Those reported here are adapted from [2] that use a supply voltage of 1.8V.

## II. SELECTING A CHARGE PUMP ARCHITECTURE

The purpose of this section is to justify the selected charge pump structure. Charge pumps have several significant characteristics such as: input voltage range, output voltage and current, internal capacitor values, oscillator frequency, and output voltage ripple. These characteristics are determined by the charge pump structure, and three (3) main classes are considered: the voltage doubler charge pump, the 'conventional' Dickson charge pump and the single cascade charge pump.

### *A. The Voltage Doubler Cascade Charge Pump*

Several different voltage doubler structures have been reported [5] such as the two-phase voltage doubler (TPVD), the Makowski charge pump and the multi-phase voltage doubler (MPVD). Those circuits generally have the best output ripple on the market, with values in the range of few hundred milliVolts or less. High gain structures are derived by cascading a basic circuit stage as shown in fig.1. Each stage produces a constant multiplicative voltage gain. The output voltage of each stage increases until the final voltage of $2xV_{IN}$ has been reached by using the output voltage of each stage as the input voltage of the next stage. Also, multiphase charge pumps with voltage gain of $2^n$ requires $2n$ clock signals to control those switches.

For large number of stages, this kind of architecture is not only impractical, since 2 clock signals need to be generated for each new stage, but also the output voltage at each stage must be lower than the breakdown voltages of CMOS drain/substrate junctions and gate oxides. Since we target high number of stages (>10) and higher voltages then the typical 12V gate oxide breakdown, this architecture is not appropriate for our specifications.

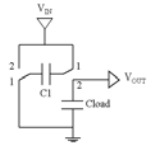


Figure 1 – Voltage doubler circuit using a two-phase clock generator

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### B. *The Dickson and Single Cascade Charge Pump*

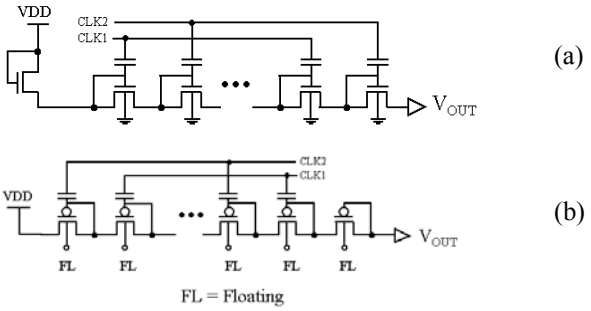


Figure 2 – Dickson ″conventional'' charge pump (a) and a floating well single cascade charge pump circuit (b)

The Dickson charge pump and single cascade charge pump, shown in fig. 2, are derived from the ideal diode charge pump architecture. Both circuits output voltage obey equation (1) that can be simplified as in equation (2)

$$V_{out} = V_{DD} - V_{th}(0) + \sum_{i=1}^{n} [\, \alpha V_{DD} - V_{th}(i)] \qquad (1)$$

$$V_{out} = V_{DD} + n\,(V_{DD}-V_{th}) \qquad (2)$$

The term $V_{DD}$-$V_{th}$ is called the voltage gain per unit stage. Note that this gain is additive and not multiplicative as in the voltage doubler architecture. In the Dickson charge pump, as the voltage of each stage increases, the threshold voltage of the diode-connected MOSFET increases due to body effect, and the voltage gain decreases as the number of stages increases. This effect is not present with the single cascade architecture. For large number of stages (>10), the Dickson charge pump has an average voltage gain of $0.25*V_{DD}$, while the single cascade circuit produces an average gain of $0.5*V_{DD}$.

### C. *The Pelliconi Cascade Charge Pump*

The Pelliconi cascade charge pump architecture proposed in [2] is shown in figure 3. It obeys equations (1) and (2). Its voltage gain is additive and not multiplicative as stipulated in [2].

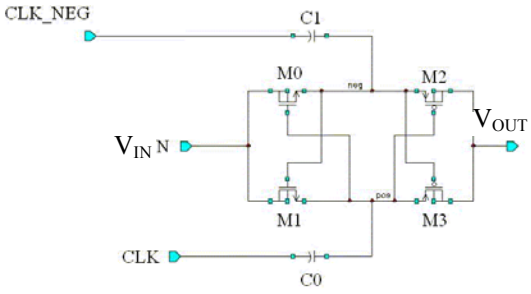


Figure 3 – Pelliconi cascade charge pump architecture

This architecture has been chosen for the following reasons. First, as the single cascade charge pump, the body effect is controlled by connecting each devices substrate to its source. In a cascade configuration, each source/substrate has a different voltage, so transistors of the same type in each stage must be in a well isolated from the well of the other stages. By having independent wells, the leakage currents are confined to respective stage and device type. The second reason for selecting this circuit is its high voltage gain. It is higher than the gain of any other additive architecture. It can reach an average of $0.9*V_{DD}$ as measured in [2]. Its simple clocking make this circuit interesting since it operates with a simple 2-phase non-overlapping clock generator. Also, its output ripples is comparable to the ripple produced by voltage doublers, as measured in [2], and it makes this circuit very attractive.

While the voltage doubler architectures exhibit a logarithmic growth of the number of devices used with the number of stages, the Dickson charge pump, the single cascade charge pump and the Pelliconi architecture show a linear growth of the number of devices. However, since the voltage gain for the Pelliconi architecture is 2.6 times higher than the gain of a Dickson charge pump, and almost twice that of a single cascade charge pump, the number of stages needed to reach a specific output voltage is reduced. This reduces the parasitic capacitances introduced in the circuit. Another great advantage is that the last stage capacitance is the same as the other stages, and no specific output stage capacitor is needed [7]. Finally, this architecture is completely symmetrical and it can also be used for negative voltage generation.

## III. MANUFACTURABILITY

The technology used is DALSA 0.8µm 5V/HV CMOS/DMOS process, with three metal layers and triple wells. A simplified process cross-sectional view is shown in figure 4. This process has been selected because it can isolate the N-Well sections from each other by using an additional mask call HV_Def, and isolated wells can be polarized at any voltage that respects junction breakdowns. Such isolated N-Well sections can be floated up to 55V above the substrate potential.

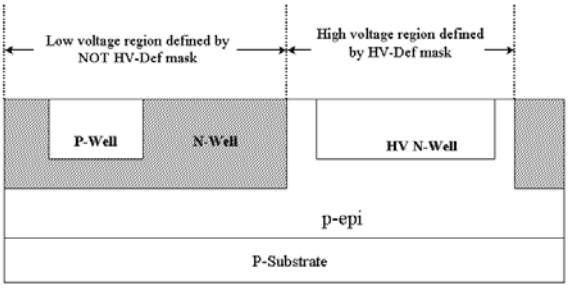


Figure 4 – Simplified cross-section view of DALSA Semiconductor 0.8µm 5V/HV CMOS/DMOS process

## IV. DESIGN AND IMPLEMENTATION OF THE SELECTED CHARGE PUMP

This section presents a charge pump that achieves good performance using low frequency clocks and small capacitors. The charge pump configuration proposed in [2] was adapted to DALSA 0.8µm CMOS/DMOS technology. Optimisation of this circuit and the obtained results are discussed in the following sections.

### *A. Charge Pump Operation and Implementation*

The adopted charge pump circuit is shown in Fig. 3. This circuit is using only standard CMOS transistors despite the fact that it is built with a high voltage process. This circuit is an excellent match to the features of the selected process. Since the target clock frequency is 10-20MHz, low-threshold CMOS transistors provide fast switching and minimize parasitic capacitances, which is desirable to increase individual stage gain. All transistors must be carefully dimensioned so that at every clock cycle, the power transfer is optimal and the voltage drop at each capacitor is minimal. The bulk of these transistors are connected respectively at $V_{IN}$ for the P-Well and at $V_{OUT}$ for the N-Well, as shown in fig.5. Since each individual bulk has no potential difference with respect to the sources of transistors in each stage, the body effect that can reduce stage gain is neutralized. To maximize the voltage difference between $V_{IN}$ and $V_{OUT}$ of each stage, while operating reliably, the input supply and the amplitude of clock pulses is set to 5V. This voltage respects the 12V gate oxide breakdown, and the 15V P-Well/N-Well junction breakdown of the process. The maximal output voltage is limited to first, capacitor oxide breakdown and secondly, to P-epi/N-Well junction breakdown. The first constraint has been solved by using stacked poly1-metal1-metal2 capacitors that can sustain voltages up to 450V. Let us now analyze how the circuit operates. In reference to figure 3, during the first half cycle, clk=VDD=5V, clk_neg=0V. Initially, if both C0 and C1 are completely discharged, M0 and M3 are on, M1 and M2 are off. In that case C1 charges and C0 discharges. The charge on C1 comes from $V_{IN}$ and the charge flowing to the output comes from CLK through C0. During the second half cycle, clk=0V, clk_neg=VDD, and the converse operation takes place, with C0 charging and $V_{OUT}$ being charged from CLK_NEG through C1. This process gradually charges capacitors C0 and C1. In the limit, both C1 and C0 charge to an asymptotic level of $V_{IN}$. If the load and parasitic capacitances are negligible, the gain per stage approaches a limit equal to the amplitude of the clock pulses. When parasitic capacitance is considered and some load current is drawn, the final voltage gain is determined by

$$\Delta V = VDD \bullet C/ (C + C_{par}) - R_{out} \bullet I_{out} \quad (3)$$

$$\text{Where} \quad R_{out} = 1/f \bullet C + R_{on} \quad (4)$$

Where C=C0=C1, $C_{par}$ is the parasitic capacitances, $R_{out}$ is the stage output resistance and $R_{on}$ is the on-resistance of the transistors. The value of internal capacitors and the number of stages needed are the most critical factors when determining the final area. In general, the capacitor value can be reduced by increasing the clock frequency; however the efficiency decreases as the frequency increases. It should also be noted that the capacitor value, combined with the frequency, dictates the number of stages needed to produce the desired output value. Based on simulations, figure 6 shows the relation between the capacitor value, the oscillator frequency and the number of stages for a fixed output voltage and current.

For our purpose, two charge pump circuits were implemented. They have the same architecture, the same transistor dimensions and capacitance values, only the capacitor structure is changed. A +20V output voltage charge pump was implemented using poly1-poly2 capacitors and a +50 V pump uses stacked poly1-metal1-metal2 capacitors. The +20V circuit will be used as a reference to compare voltage gain drop as the number of stages increases, and to allow comparing with results presented in [2], knowing that our 20V circuit and the one in [2] have the same number of stages.

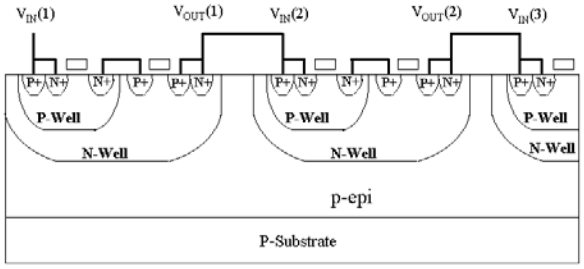


Figure 5 – Simplified cross-section view of charge pump physical implementation where $V_{IN}(1)$ is the input voltage at stage 1

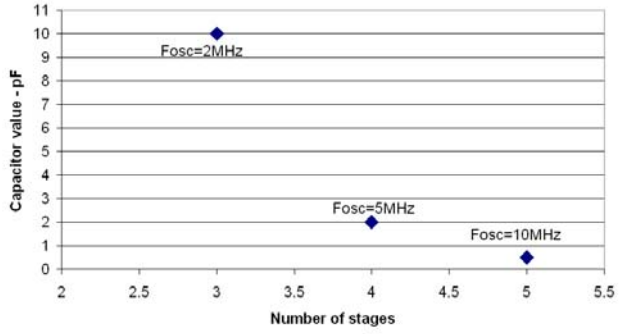


Figure 6 – Relation between the capacitor values, the number of stages and the oscillator frequencies

## V. MEASURED RESULTS AND DISCUSSION

Two charge pump circuits were implemented. The first, circuit A, uses two-polysilicon-plate capacitors and five (5) stages. It produces an output voltage of +20V, which is close to the breakdown voltage of the capacitor oxide (~25V). The second, circuit B, uses stacked poly1-metal1-metal2 capacitors and sixteen (16) stages. It produces an output voltage of +50V, which is close to the N-Well/P-epi junction breakdown (~55V). These circuits were tested with a 28pF capacitive load. Table 1 summarizes our measured results and compares them with competitive results reported in [2]. Both charge pump circuits have an output voltage ripple of 400mV. Those ripples could be reduced if an additional capacitive output load was added or by increasing the clock frequency. The power-up delay measured for circuit A is 250µs as shown in fig. 7. Figure 8 shows a die photograph of the two circuits. Circuit A (bottom) consumes ~30K$\mu m^2$ while Circuit B (top) occupies approximately 11 times the area of circuit A and has 3.2 times more stages. From table 1, the voltage gain of circuit A is equal to 0.6*VDD. By lowering the input and supply voltage to 1.8V, the voltage gain is equal to 0.75*VDD which is less then the 0.9*VDD measured in [2]. This difference is due to a compromise between area and performance. A higher voltage gain could be achieved if higher capacitor values had been selected as in fig. 6. Also, interconnects are made in metal2 to reduce parasitics, but the process cannot match the low parasitics feasible with a multi-metal layers submicron process.

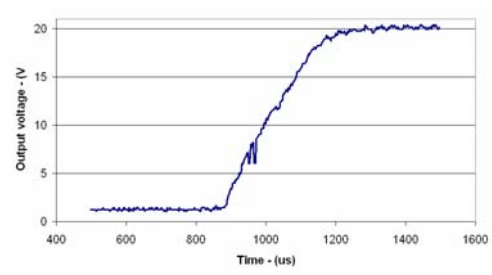


Figure 7 – Circuit A Power-UP sequence

Table 1 –Measured characteristics of various charge pumps

| Parameter | Circuit A | Circuit B | [2] | Units |
|---|---|---|---|---|
| Geometry | 0.8 | 0.8 | 0.18 | µm |
| Input voltage | 5.0 | 5.0 | 1.8 | Volts |
| Output voltage | 20.0 | 50.0 | 10.1 | Volts |
| Number of stages | 5 | 16 | 5 | -- |
| Voltage gain per stage | 3 | 2.8 | 1.7 | Volts |
| Oscillator frequency | 10 | 10 | 100 | MHz |
| Output voltage ripples | 400 | 400 | 400 | mV |
| Output current | 25 | 50 | 350 | µA |
| Area | 30K | 330K | -- | $\mu m^2$ |

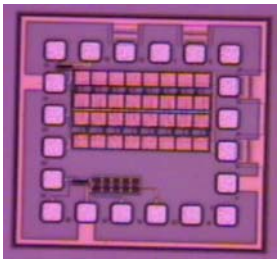

Figure 8 – Micro-photograph of two charge pump circuits in a single die

## VI. CONCLUSION

The high performance HV CMOS charge pump circuits presented in this paper offer simple and efficient solutions suitable for telecom, automotive and MEMS applications. Additive voltage gain per stage above 2.8V is reported. Also, the maximum output voltage reaches +50V from a +5V input supply, using only low-voltage CMOS devices of a 0.8µm CMOS/DMOS DALSA Semiconductor technology. These circuits were found to remain functional when the supply and input voltage ranges from +2V to +5V supply.

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