03-TDEN_FIRDAC

High Accuracy Low OOBN ΣΔ DAC

Features

- Excellent THD performance:
  THD+N < -110 dB (20 - 20kHz)
- Low out-of-band-noise (OOBN): -60 dBFS
- Dynamic range: up to 120 dB (20 - 20kHz)
- Good matching properties
- Robust against clock jitter
- Insensitive to inter symbol interference (ISI)
- Multi-bit advantages with a single bit modulator
- Silicon proven in CMOS 140nm and 180nm
- Multiple configurations:
  - Push-Pull or Pull
  - Single-ended or differential
- High output compliance: no direct need for buffer
- Area: 0.14 mm^2 per channel

Applications

- High accuracy digital-to-analog conversion with low OOBN
- Signal generation for class-D and class-AB amplifiers
- Audio subsystem
- Makes a complete audio front-end system in combination with up-sampling filters and digital audio interface

Description

The AXIOM_FIRDAC is a high accuracy sigma-delta digital-to-analog converter. The low out-of-band-noise (OOBN) down to -60dBFS makes the converter ideally suited for application with strict OOBN requirements. The PWM modulator is a special type of 1-bit sigma-delta modulator that produces a pulse width modulated (PWM) signal with a fixed repetition frequency (see PWMMOD datasheet). A fixed repetition rate makes the output signal insensitive to non-linear inter symbol interference (ISI).

The semi-digital FIR filter topology of the FIRDAC makes the FIRDAC behave as a multi-bit DAC. This gives the converter its excellent OOBN and makes the system robust against clock jitter and other error sources typically associated with 1-bit converters while maintaining excellent THD and good matching properties.
The AXIOM_FIRDAC is ideally suited for digital-to-analog conversion in front of (analog) class-D or class-AB amplifiers. Additionally this IP can be delivered together with up-sampling and interpolation filters as signal pre-processing. The design and layout of the FIRDAC is a highly automated process, easy to scale and good portable to several CMOS technologies.

The following specifications and measurement results are based on a silicon implementation of the IP. Specifications can be modified to meet customer requirements. Porting to several technologies is possible in a contract development project.

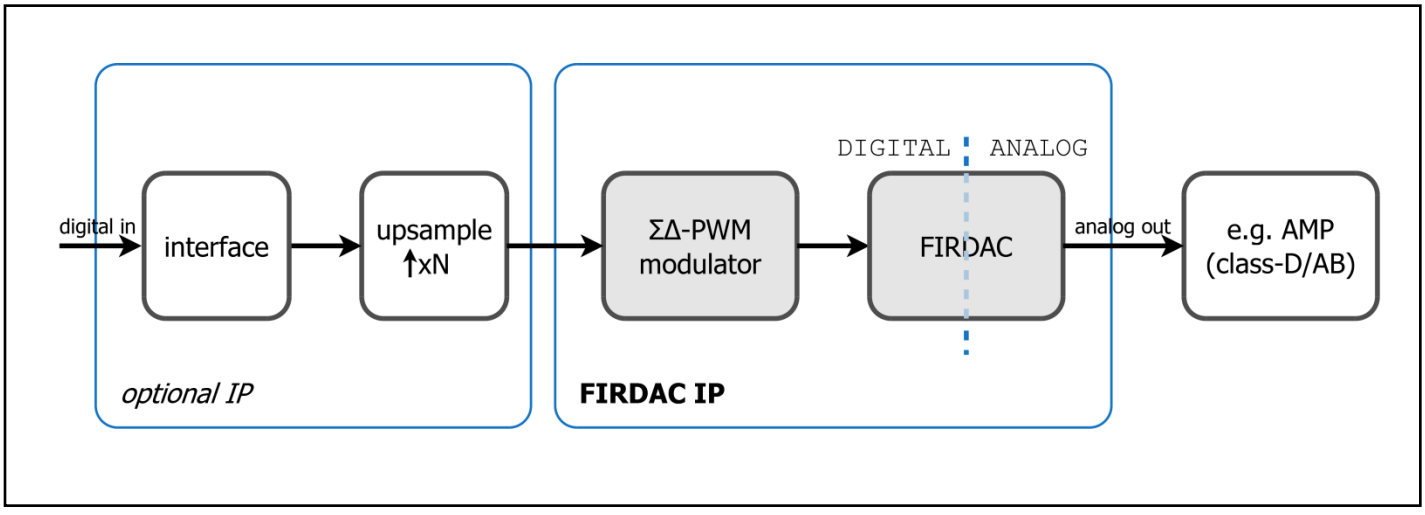

Figure 1 – Block diagram of the FIRDAC IP including optional pre-processing IP.

Specifications[1]

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
TECHNOLOGY					
Tech	NXP C14 0.14µm CMOS technology XFAB XP018 0.18µm CMOS technology		0.14 0.18		µm
Area	Approximate area for one channel[2]: Analog FIRDAC Digital PWM modulator Analog reference area Digital area (optional IP for one channel)		0.14 0.12 0.018 0.022 0.182		mm^2
TEMPERATURE					
T_{OP}	Functional operating temperature	-40	25	150	ºC
ELECTRICAL					
V_{DDA}	Analog supply voltage		1.8		V
I_{PD}	Power down current		1		µA
$I_{FIRDAC/CH}$	FIRDAC supply current per channel		0.66		mA
INPUTS					
f_S	Base input sample rate		44.1		kHz
f_{CLK}	System clock frequency		$256*f_S$		
N	Input data word-length		24		bits
I_{REF}	Reference current input		0.2		mA
PERFORMANCE					
DR	Dynamic Range[3] - Un-weighted - A-weighted[4]		 114 116		 dB dBA
SINAD	Signal to Noise And Distortion ratio[5] - Un-weighted - A-weighted		 >102 >104		 dB dBA
THD	- 100Hz 0dBFS - 1kHz 0dBFS - 10KHz 0dBFS		-113 -113 -114		dB dB dB
OOBN	Integrated out-of-band-noise[6]		-60		dBFS
ΔG	Inter-channel gain variation			0.1	dB
X_{TALK}	Channel Crosstalk	-100			dB
R_P	Pass-band ripple (peaking at 20kHz)		0.2		dB
PSR	Power supply rejection (measured with -60dBFS 1kHz input) - 217Hz square wave 200mV_{PP} - 1.5kHz 200mV_{PP} at V_{DDA} - 19.5kHz 200mV_{PP} at V_{DDA} - 766.5kHz 200mV_{PP} at V_{DDA}		 -100 -100 -101 <-110		 dBFS dBFS dBFS dBFS

Table 1 – Specifications of the FIRDAC

[1] Specifications are based on measurements performed on our first 2-channel pull FIRDAC. Note that multiple versions with a range of DR performances is validated on silicon and availalble with dedicated specification tables
[2] Note that the analog reference is shared for multiple channels and the optional interface IP incl. RAM and ROM is included in the digital area.
[3] Test condition: SNR measurement @ -60 dBFS input over 20Hz to 20kHz bandwidth; DR = SNR+60 dB.
[4] For this measurement an A-weighting filter has been used
[5] Measured with 0dBFS input signal over complete audio band
[6] Integrated over a band from 20kHz to 500kHz

Measured Performance

The following measurements are performed on a Pull FIRDAC connected with resistors to the supply used as current to voltage converters. The measurement equipment used is a Rhode & Schwarz UPL audio analyzer.

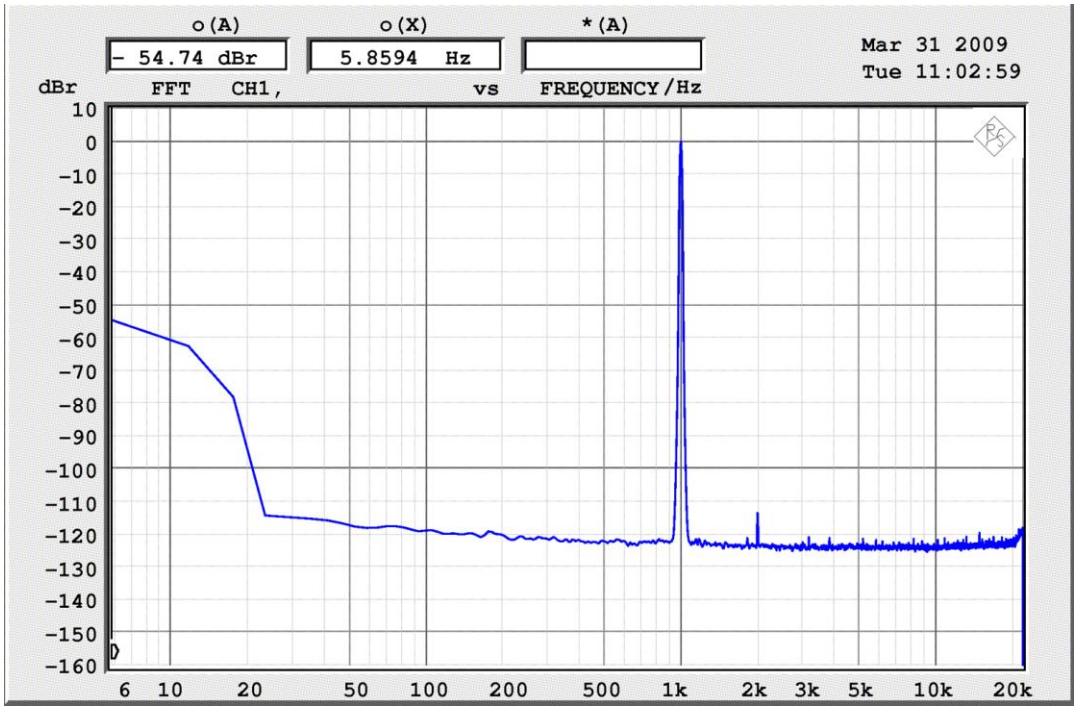

Figure 2 – Output spectrum of the FIRDAC with a single tone @ 1kHz 0dBFS. THD < -110 dBFS.

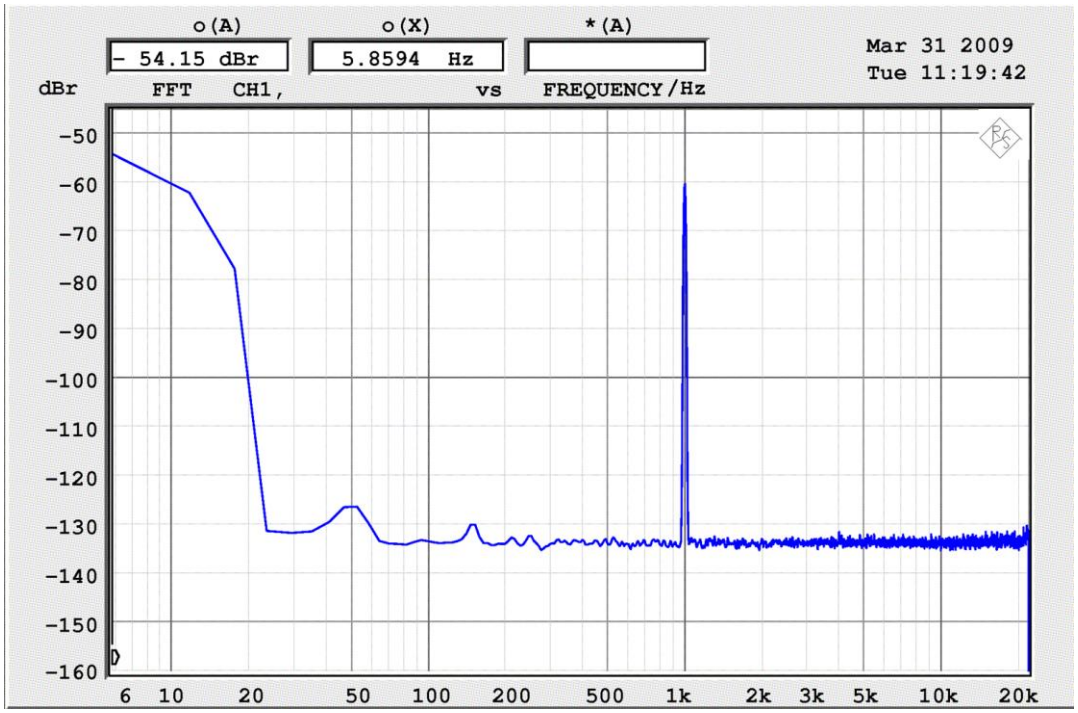

Figure 3 – Output spectrum of the FIRDAC with a single tone of 1kHz.

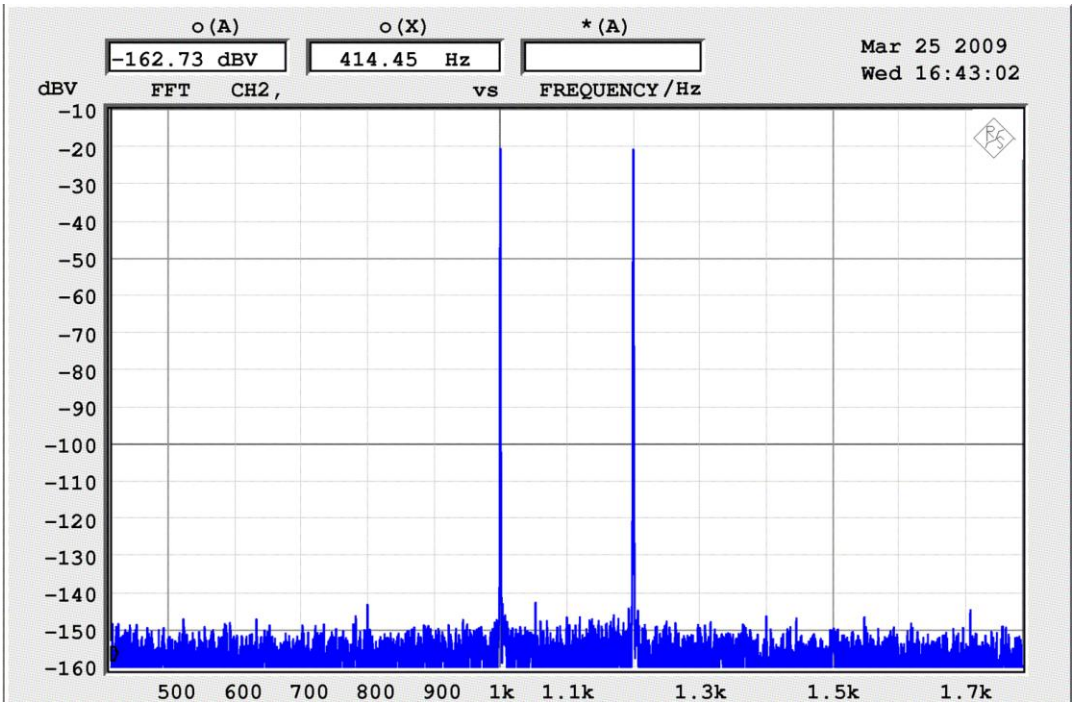

Figure 4 – Two-tone intermodulation 1kHz and 1.2kHz; both input tones at -20dBFS. Intermodulation tone hardly detectable @ 800 Hz.

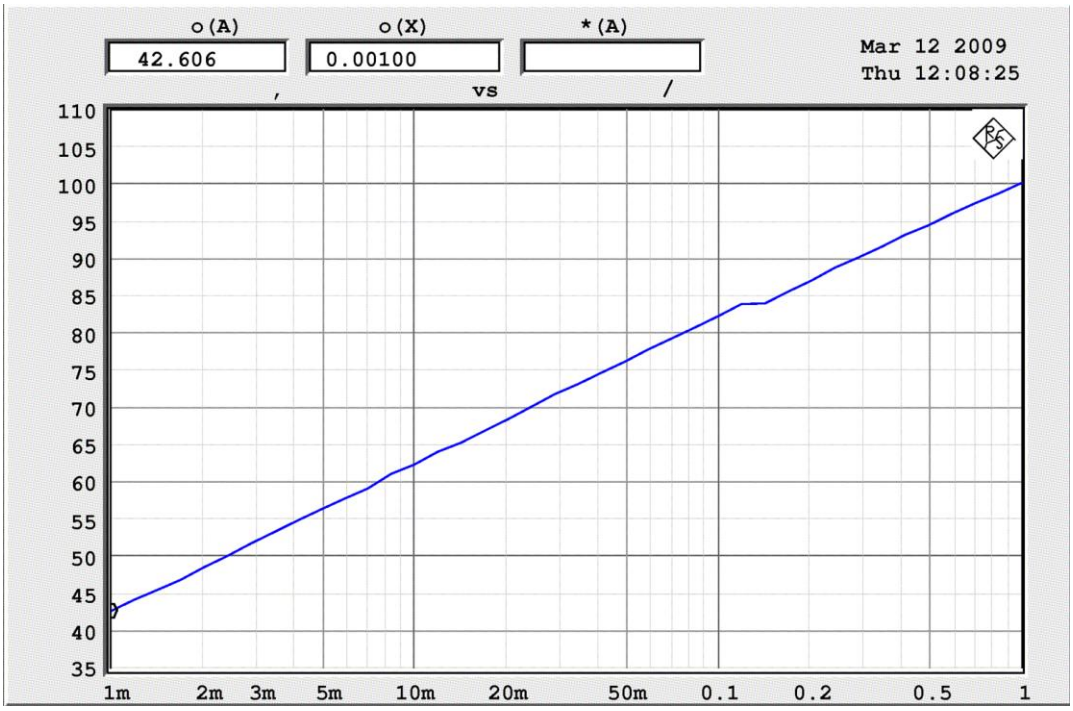

Figure 5 – SINAD vs. input fraction; no weighting filter (irregularity @input 0.12 due to range switching of the audio analyzer)

Applications

The FIRDAC IP can be delivered featuring different configurations. Depending on the need of the customer and its application the FIRDAC IP can be delivered with the following configurations:

- Push-Pull or Pull only
- Single-ended or differential

This section will give two application examples that have been realized with the FIRDAC IP using these configurations.

Push-Pull FIRDAC: class-AB HPA driver

In the application as shown in Figure 6 the FIRDAC is used to drive a headphone amplifier (HPA). This can be done very elegantly by using a push and a pull mechanism (two types of FIRDACs combined) where the lower (NMOST) FIRDAC purely converts the differential signal and the upper (PMOST) FIRDAC purely convert a common-mode signal. The resulting current drives a HPA with current feedback. This way the push-pull configuration can be used to bias the HPA by controlling the FIRDAC such that VCM stays at fixed reference voltage while at the same time converting the actual signal and applying it to the HPA.

Advantages compared to traditional converters

Advantages of this system over a system with a DAC where the HPA is biased by a separate and fixed current source:

- Usually 1/f noise of a fixed current source needs to be cancelled by chopping. The FIRDAC inherently has a “chopping-like” behavior because of its switching current sources.
- Since both differential input signal and bias signal for the HPA are controlled by the FIRDAC, pop-free start-up can be simplified.

Next to the above advantages this system also comes with the general FIRDAC benefits:

- Low out-of-band noise (OOBN) without the need of a separate low-pass filter.
- Robust against clock jitter and other error sources which are typically associated with 1-bit converters.
- The special type of PWM modulator makes the system insensitive to inter symbol interference (ISI).
- Excellent THD and good matching properties.

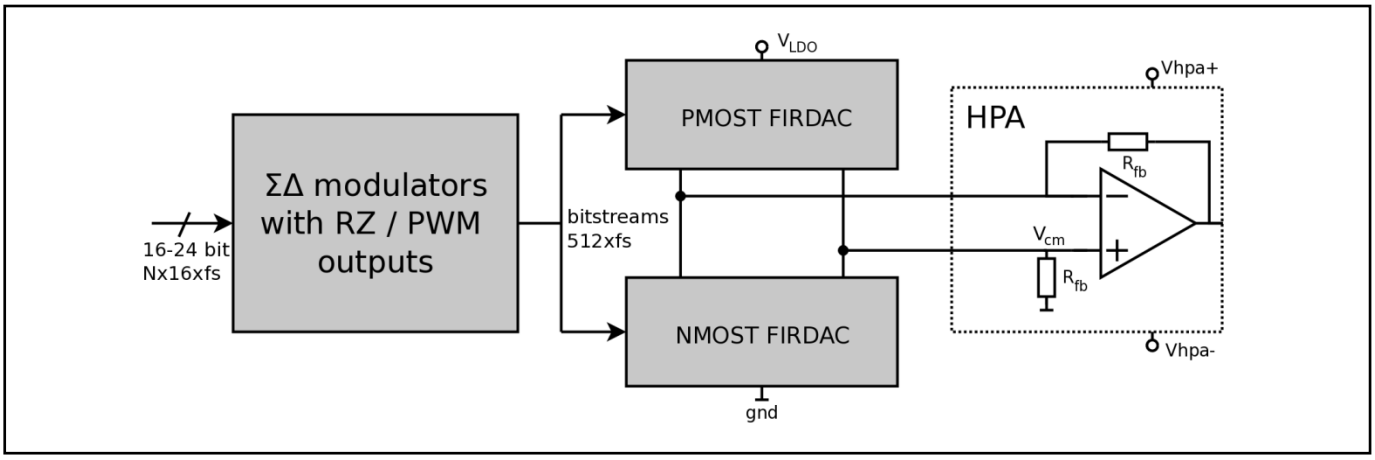

Figure 6 – Push-Pull FIRDAC in front of a class-AB headphone amplifier.

FIRDAC as input DAC for class-D power amplifier

The application where the FIRDAC is used in front of an analog class-D power amplifier is shown in Figure 7. It comprehends a full audio front-end for class-D power amplification. The first stage contains a digital serial audio interface, in an I2S-like format, and up-sampling from 1fs to 2fs and 4fs including volume control and mute. The following digital DAC processing stage contains an IIR filter to further up-sample to the preferred oversampling ratio for the 1-bit PWM ΣΔ modulator. The actual conversion takes place at the DAC stage where the FIRDAC converts the PWM signal to a multi-bit like analog signal with build in semi-digital FIR filtering.

Advantages compared to traditional converters

Compared to a system with a traditional converter this system comes will the following advantages:

- Low out-of-band noise (OOBN) without the need of a separate low-pass filter.
- Robust against clock jitter and other error sources which are typically associated bit 1-bit converters.
- The special type of PWM modulator makes the system insensitive to inter symbol interference (ISI).
- Excellent THD and good matching properties.

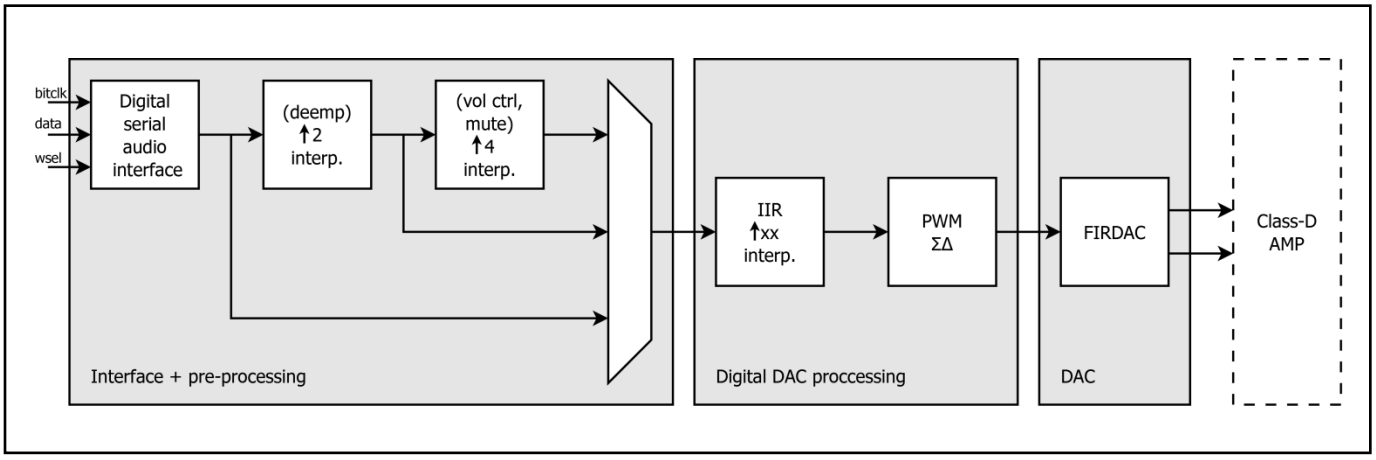

Figure 7 – System overview of the FIRDAC for an analog class-D power amplifier.

Delivery

The IP deliverables consist of a GDS file, a behavioral model, a netlist, a datasheet and integration documentation. The product can be delivered as a single IP component for customer integration or Teledyne Axiom IC engineers can integrate the product as part of a SoC engagement.

VIEW	FILE TYPE	DESCRIPTION
Behavioral model	VHDL / Verilog / Simulink	Behavioral model of the IP which can be used for simulation purposes
Netlist	CDL	Netlist for LVS checks
Layout	GDS2	Layout database
Abstract	LEF	Abstract view with layout boundaries and pinning information
Checks	DRC/LVS/ANT	Verification checks results performed on the layout
RTL	VHDL	VHDL code
Timing & interface	SDC & LIB	Timing constrains and interface information
Design documentation	PDF	Datasheet, specifications and simulation results
Integration documentation	PDF	Interface description for integration

Table 2 – Deliverables of the IP

Revision history

REVISON	DATE	REASON FOR REVISION
F3	2014-02-11	Release for publication on the website
F4	2017-11-07	Added optional features from our latest 120dB variant

Table 3 – Document revision history

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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